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(54) Title: DIELECTRIC BARRIER LAYER FILMS

(57) Abstract: In accordance with the present invention, a dielectric barrier layer is presented. A barrier layer according to the present invention includes a densified amorphous dielectric layer deposited on a substrate by pulsed-DC, substrate biased physical vapor deposition, wherein the densified amorphous dielectric layer is a barrier layer. A method of forming a barrier layer according to the present inventions includes providing a substrate and depositing a highly densified, amorphous, dielectric material over the substrate in a pulsed-dc, biased, wide target physical vapor deposition process. Further, the process can include performing a soft-metal breath treatment on the substrate. Such barrier layers can be utilized as electrical layers, optical layers, immunological layers, or tribological layers.

TITLE OF THE INVENTION

DIELECTRIC BARRIER LAYER FILMS

RELATED APPLICATIONS

[001] The present application claims priority to U.S. Provisional Application 60/451,178, "Dielectric Barrier Film," filed on February 27, 2003, by Richard E. Demaray, Mukundan Narasimhan, and Hongmei Zhang, herein incorporated by reference in its entirety, and to U.S. Provisional Application 60/506,128, "Indium Nucleation Layer," filed on September 25, 2003, by Mukundan Narasimhan and Peter Brooks, herein incorporated by reference in its entirety.

BACKGROUND

1. Field of the Invention

[002] The present invention is related to dielectric barrier films and, in particular, dielectric barrier films formed from high-density optical material layers for utilization in optical, electrical, tribological, and bio-implantable devices.

2. Discussion of Related Art

[003] Dielectric barrier layers are becoming increasingly important as protective layers for organic light emitting diodes (OLEDs) and other optical or opto-electronic devices. Typically, dielectric barrier layers are deposited thin films with the appropriate electrical, physical, and optical properties to protect and enhance the operation of other devices. Dielectric barrier layers can be utilized in optical, electrical, or tribological devices. For example, touch screen displays require

optically transparent protective layers to protect against transmission of atmospheric contaminants as well as to protect against physical wear.

[004] Many thin film deposition technologies that may be utilized to form such dielectric layers include some form of ion densification or substrate bias densification. The densification process eliminates the columnar thin film structure that is typical of vacuum deposited chemical vapor (CVD) or physical vapor deposition (PVD) thin films. It is well known that such densification can be achieved by a secondary ion source arranged to "bombard" the film during deposition. *See, e.g.,* W. Essinger "Ion sources for ion beam assisted thin film deposition," Rev. Sci. Instruments (63) 11-5217 (1992). *See, also,* Hrvoje Zorc, et al. Proceedings of the Society of Vacuum Coaters, 41st Annual Technical Conference Proceedings, 243-247, 1998, which discusses the effects of moisture exposure on wavelength shift for electron beam evaporated films (e-beams). In particular, Zorc et al. demonstrated a factor of 15 or so improvement in wavelength shift for electron beam evaporated films (e-beam) as compared to e-beam films deposited with a directed ion beam source after exposure to 30% humidity at 25 °C.

[005] D. E. Morton, et al. demonstrated wide-band dielectric pass filters comprised of alternating layers of SiO_2 and TiO_2 deposited using a "cold cathode ion source" to produce oxygen ions for the purpose of providing "moisture stable stacks of dense optical films of silicon dioxide as the low index material and either titanium dioxide, tantalum pentoxide or niobium pentoxide." D. E. Morton, et al. Proceedings of the Society of Vacuum Coaters, 41st annual Technical Conference, April 18-23, 1998. The results described by Morton, et al., indicated that room temperature

resistance to humidity up to 100% humidity was attained, as measured by the optical performance of single dielectric layers deposited on substrates mounted on a rotating platen. Optical extinction coefficients for the six samples tested in Morton, et al., varied from 0.1 to 1.6 ppt, indicating the presence of significant concentrations of defects or absorption centers in the dielectric layers. Additionally, no film thickness or film thickness uniformity data was reported by Morton, et al., for ion beam energies between 134 and 632 Volts and ion beam current up to 5 amps. Morton, et al., therefore fail to describe a film that would operate as a good barrier layer for optical devices.

[006] Self biased physical vapor deposition, such as ion coating or activated reactive deposition, are well-known means of providing hard wear resistant coatings. However, these coatings are either deposited at several hundred Volts of bias voltage and form penetrating surface treatments with the ion flux penetrating the surface to react with the substrate material, or they are ion assisted for the purpose of decreasing the columnar structure of the film. A "filtered cathodic vacuum arc" (FCVA-reference - http://www.nanofilm-systems.com /eng/fcva_technology.htm) has been used to form a dense film from an ion flux. In this case, ions are created and separated from the neutral vapor flux by a magnetic vector so that only species having a positive charge impinge the substrate. The bias voltage can be preset so that average translational energy ranges from about 50 to several hundred Volts are available. Lower ion energies are not reported due to the problem of extracting and directing a lower energy ion flux with a useful space charge density. Although quite rough due to re-sputtering at the high ion energies, hard protective layers of alumina,

and other materials such as tetrahedral carbon, can be deposited with this process on cutting tools and twist drills with commercial levels of utility. Due to the limitation of the coating species to the ion flux, coating rates are low. The best or hardest carbon films are often deposited with the lowest rate of deposition, e.g., 0.3 nanometers per second on substrates up to 12" in diameter.

[007] Transmission of a ZnO film deposited by FCVA at 600 nm wavelength is increased from about 50% at room temperature to above 80% for single films by increasing the temperature of deposition to above 230 °C, with the best transmission at 600 nm of about 90% at a deposition temperature of 430 °C and a substrate bias voltage not greater than about 50 Volts. This high temperature processing indicates the use of a thermal anneal process for repair of ion-induced damage to the films. For FCVA deposition with a 200 Volt bias the transmission is much reduced. FCVA films deposited in this fashion have been shown to be polycrystalline. The defect structures exhibited in the FCVA layer are too large for formation of effective optical barrier layers. Additionally, ion sputtering of crystalline films is dependent on the crystal orientation, leading to higher surface roughness. Defect structures formed in a protective layer can degrade the optical quality of the layer and also provide paths for diffusion of atmospheric contaminations through the layer, compromising the protective properties of the layer.

[008] Ion biased films have shown significant progress toward the goal of providing a satisfactory barrier for protection of electronic and optical films, such as, for example, photovoltaic, semiconducting and electroluminescent films. Particularly organic light emitting diodes, which utilize calcium or other very reactive metal

doped electrodes and other hydroscopic or reactive materials, can be protected by such films. However, the most biased process to date, the filtered Cathodic Vacuum Arc Coating Technology or FCVAC process, is reported to produce films with a particle density greater than about 1 defect per square centimeter. It may be that the high resputtering rate at the high voltages used in this process cause surface roughening. Certainly, the presence of a particle represents a defect through which diffusion of water vapor or oxygen can proceed. Also, the roughness of the surface formed by the FCVAC process impacts the stress and morphology and also the transparency and the uniformity of the index of refraction. The resputtered film may flake from the process chamber shields or be drawn to the film surface by the large electrostatic field present in an ion beam process. In any case, the particle defect density for particles greater than the film thickness also determines pin hole density or other defects caused by discontinuous deposition of the film because line of sight films can not coat over a particle that is larger than the thickness of the film, let alone a particle many times greater in size than the thickness of the film.

[009] In the case of ion-bias or self-bias energies exceeding several electron volts, the translational energy of the ion participating in the bias process can exceed the chemical binding energy of the film. The impacting ion, then, can either forward scatter atoms of the existing film or back sputter atoms of the existing film. Likewise, the participating ion can be adsorbed into the growing film or it can also scatter or absorb from the film surface. Sputtering of the existing film and scattering from the existing film are both favored at incoming angles of about 45° from the horizontal. In most ion coating processes, the ion beam is directed at a normal incidence to the

surface to be coated. However, as noted, at ion energies exceeding the chemical threshold, and particularly at energies exceeding 20 Volts or so, damage to the film or the substrate resulting from the ion energy in excess of the chemical binding energy is significant, and results in surface roughness, increased optical absorption characteristics, and creation of defects.

[010] In the case of the FCVA process, roughness is an increasing function of the film thickness, increasing from about 0.2 nanometers roughness for a 50 nanometer film to about 3 nanometers for a 400 nanometer Cu film indicating substantial roughening of the polycrystalline copper surface due to differential sputtering by the self biased incoming copper ions. Such a film will scatter light, particularly at the interface between two layers of different refractive index. To date, barrier or dielectric properties of FCVA produced films have not been found.

[011] Charging of the deposited film is also a particular problem with ion beam deposited dielectrics. To date, no low temperature dielectric and also no ion beam dielectric is known that has ever been shown to provide the electrical quality required for a transistor gate layer, for example. The ion beams embed charged ions in the film, leading to large negative flat band voltages and fields that can not be passivated at temperatures below about 450 °C. The surface charge of the dielectric layer results in slow accumulation of capacitance, preventing the sharp onset of conduction in a transistor application. Consequently, no as-deposited low temperature dielectric, biased or unbiased, has been proposed for low temperature transistor applications or is known at this time.

[012] Therefore, there is a need for high quality, dense dielectric layers for utilization as barrier layers in optical, electrical, tribological, and biomedical applications.

SUMMARY

[013] In accordance with the present invention, one or more dielectric layers formed from layers of metal-oxide materials deposited by a pulsed, biased, wide area physical vapor deposition process are presented. A dielectric barrier layer according to the present invention can be formed from at least one highly densified metal oxide layer. Dielectric barriers according to the present invention can be highly densified, highly uniform, ultra smooth amorphous layers with ultra low concentrations of defects, providing for superior performance as protective layers against physical wear and atmospheric contamination of underlying structures as well as overlying structures that may be deposited to form an electrical, optical, or medical device. Barrier layers according to the present invention can also be self-protecting optical layers, electrical layers, or tribological layers that can be utilized actively in optical or electrical devices.

[014] Therefore, barrier layers according to the present invention includes a densified amorphous dielectric layer deposited on a substrate by pulsed-DC, substrate biased physical vapor deposition, wherein the densified amorphous dielectric layer is a barrier layer. Further the deposition can be performed with a wide area target. A method of forming a barrier layer according to the present inventions includes providing a substrate and depositing a highly densified, amorphous, dielectric material over the substrate in a pulsed-dc, biased, wide target physical vapor deposition

process. Further, the process can include performing a soft-metal breath treatment on the substrate.

[015] Dielectric barrier stacks can include any number of individual layers including one or more barrier layers according to the present invention. In some embodiments, the individual barrier layers can be optical layers. Typically, alternating layers of low and high index of refractory metal oxide materials can be arranged to form anti-reflective or reflective coatings in optical devices, for example. As such, dielectric barriers according to the present invention provide a protective function as well as being a functional part of an optical device. In some embodiments of the invention, for example, dielectric barriers according to the present invention can be utilized in cavity enhanced LED applications, or in formation and protection of transistor structures. Additionally, the beneficial dielectric properties of some embodiments of barrier layers according to the present invention can be utilized as electrical layers to form resistors or capacitive dielectrics.

[016] In some embodiments, a soft metal (e.g., indium) breath treatment can be utilized before deposition of a barrier layer. Such a breath treatment is shown to significantly improve surface roughness and enhance WVTR characteristics for embodiments of barrier layers according to the present invention.

[017] These and other embodiments of the invention are further discussed and explained below with reference to the following Figures. It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed. Further, specific explanations or theories regarding the deposition or performance of

barrier layers or soft-metal breath treatments according to the present invention are presented for explanation only and are not to be considered limiting with respect to the scope of the present disclosure or the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[018] Figures 1A and 1B illustrate a deposition apparatus for depositing barrier layer films according to the present invention.

[019] Figure 1C illustrates a barrier layer deposited on a substrate according to embodiments of the present invention.

[020] Figures 2A, 2B, 2C, 2D, 2E and 2F illustrate examples of devices with dielectric stacks of barrier layers according to embodiments of the present invention.

[021] Figure 3 shows a microcavity enhanced LED structure utilizing dielectric stacks of barrier layers according to embodiments of the present invention.

[022] Figure 4 shows a bottom gate transistor device with a dielectric stack of barrier layers according to embodiments of the present invention.

[023] Figure 5 shows a top gate transistor device with a dielectric stack of barrier layers according to embodiments of the present invention.

[024] Figure 6 shows an example of a microcavity enhanced LED structure similar to that shown in Figure 3 further protected by a dielectric stack of barrier layers according to embodiments of the present invention.

[025] Figure 7 shows another example of a microcavity enhanced LED structure similar to that shown in Figure 3 further protected by a dielectric stack of barrier layers according to embodiments of the present invention.

[026] Figure 8 shows an example TiO_2 barrier layer according to embodiments of the present invention deposited on a reactive aluminum layer after exposure to a high humidity, high temperature environment for an extended period of time.

[027] Figure 9 shows an example silica/alumina barrier layer according to embodiments of the present invention deposited on a reactive aluminum layer after exposure to a high humidity, high temperature environment for an extended period of time.

[028] Figure 10 shows an SEM photograph of a cross section of an embodiment of a dielectric stack of barrier layers according to embodiments of the present invention.

[029] Figure 11 shows transmission versus wavelength curves for various examples of dielectric stacks of barrier layers according to embodiments of the present invention.

[030] Figures 12A and 12B illustrate a single barrier layer structure deposited with and without a soft-metal breath treatment according to embodiments of the present invention.

[031] Figure 13 shows a Flexus Stress Measurement apparatus that can be utilized to test barrier layers.

[032] Figure 14 illustrates a measurement of the wafer bow using the Flexus Stress Measurement apparatus illustrated in Figure 13.

[033] Figure 15 illustrates the stress in various deposited barrier layers according to embodiments of the present invention as a function of temperature through a single temperature cycle after deposition.

[034] Figures 16A, 16B, 16C, and 16D show atomic force microscopy measurements of surface roughness for some barrier layer films according to embodiments of the present invention.

[035] Figure 17 illustrates a water vapor transmission test that can be utilized to characterize barrier layers deposited according to embodiments of the present invention.

[036] Figures 18A through 18D illustrate the effects of different In/Sn breath treatment parameters on the surface roughness of the deposited barrier layer according to the present invention.

[037] Figures 19A and 19B illustrate the effects of the substrate on surface roughness.

[038] Figure 20 illustrates a barrier layer according to the present invention that further operates as a thin film gate oxide.

[039] Figures 21A and 21B illustrate the effect of substrate composition on the surface roughness of a deposited barrier layer according to the present invention.

[040] Figures 22A and 22B illustrate that the character of the barrier layer deposition according to embodiments of the present invention effect surface roughness.

[041] In the figures, elements having the same designation have the same or similar functions.

DETAILED DESCRIPTION

[042] Barrier layers according to some embodiments of the present invention are deposited in a pulsed-dc, substrate biased, wide target physical vapor deposition process that is described further below with respect to some particular examples of such barrier layers. Some embodiments of barrier layers according to embodiments of the present invention can be characterized as highly densified, highly uniform, highly amorphous layers with particularly low defect concentrations and high surface smoothness. Further, barrier layers according to embodiments of the present invention can have beneficial optical and electrical characteristics that allow such barrier layers to be self-protecting optical or electrical layers in optical or electrical devices formed with these layers.

[043] For example, some embodiments of barrier layers according to the present invention can have excellent optical transparency characteristics. Further, the index of refraction of individual barrier layers is dependent on the material of deposition and therefore stacking of multiple barrier layers according to the present invention can result in highly controllable, and self protecting, reflecting or anti-reflecting coatings for optical devices. Additionally, barrier layers according to some embodiments of the present invention can be doped with optically active impurities to form optically active layers, which are also self-protecting. For example, depositions of rare-earth ions such as Erbium or Ytterbium can result in optical amplifiers or frequency converters.

[044] Additionally, embodiments of barrier layers according to the present invention can have highly beneficial dielectric properties and can therefore be utilized as self-protecting electrical layers. Some barrier lavers according to embodiments of

the present invention, for example, can be utilized as resistance layers. Other embodiments can be utilized as high-dielectric constant layers in capacitor devices. Embodiments of dielectrical barrier layers that are useful for such devices are further discussed below.

[045] RF sputtering of oxide films is discussed in Application Serial No. 09/903,050 (the '050 application), filed on July 10, 2001, by Demaray et al., entitled "Planar Optical Devices and Methods for Their Manufacture," assigned to the same assignee as is the present invention, herein incorporated by reference in its entirety. Further, targets that can be utilized in a reactor according to the present invention are discussed in U.S. Application serial no. 10/101,341, filed on March 16, 2002, assigned to the same assignee as is the present invention, herein incorporated by reference in its entirety. Methods of depositing oxides in a pulsed-dc, substrate biased, wide-target physical vapor deposition (PVD) process are further discussed in U.S. Application serial no. 10/101863, filed on March 16, 2002, (hereinafter referred to as "the pulsed, biased process") assigned to the same assignee as is the present application, herein incorporated by reference in its entirety.

[046] Figures 1A and 1B illustrate a reactor apparatus 10 for sputtering of material from a target 12 according to embodiments of the present invention. In some embodiments, apparatus 10 may, for example, be adapted from an AKT-1600 PVD (400 X 500 mm substrate size) system from Applied Komatsu or an AKT-4300 (600 X 720 mm substrate size) system from Applied Komatsu, Santa Clara, CA. The AKT-1600 reactor, for example, has three or four deposition chambers connected by a vacuum transport chamber. These AKT PVD reactors can be modified such that

pulsed DC power is supplied to the target and RF power is supplied to the substrate during deposition of a material film.

[047] Apparatus 10 includes a target 12 which is electrically coupled through a filter 15 to a pulsed DC power supply 14. In some embodiments, target 12 is a wide area sputter source target, which provides material to be deposited on substrate 16. Substrate 16 is positioned parallel to and opposite target 12. Target 12 functions as a cathode when power is applied to it and is equivalently termed a cathode. Application of power to target 12 creates a plasma 53 below target 12. Magnet 20 is scanned across the top of target 12. Substrate 16 is capacitively coupled to an electrode 17 through an insulator 54. Electrode 17 can be coupled to an RF power supply 18.

[048] For pulsed reactive dc magnetron sputtering, as performed by apparatus 10, the polarity of the power supplied to target 12 by power supply 14 oscillates between negative and positive potentials. During the period of positive potential, the insulating layer on the surface of target 12 is discharged and arcing is prevented. To obtain arc free deposition, the pulsing frequency of pulsed DC power supply 14 can exceed a critical frequency that can depend, at least partly, on target material, cathode current and reverse time. High quality oxide films can be made using reactive pulse DC magnetron sputtering in apparatus 10.

[049] Pulsed DC power supply 14 can be any pulsed DC power supply, for example an AE Pinnacle plus 10K by Advanced Energy, Inc. With this example supply, up to 10 kW of pulsed DC power can be supplied at a frequency of between 0 and 350 KHz. The reverse voltage is 10% of the negative target voltage. Utilization

of other power supplies will lead to different power characteristics, frequency characteristics and reverse voltage percentages. The reverse time on this embodiment of power supply 14 can be adjusted to between 0 and 5 μs.

[050] Filter 15 prevents the bias power from power supply 18 from coupling into pulsed DC power supply 14. In some embodiments, power supply 18 is a 2 MHz RF power supply and, for example, can be a Nova-25 power supply made by ENI, Colorado Springs, Co. Therefore, filter 15 is a 2 MHz band rejection filter. In some embodiments, the band-width of the filter can be approximately 100 kHz. Filter 15, therefore, prevents the 2 MHz power from the bias to substrate 16 from damaging power supply 18.

[051] However, both RF and pulsed DC deposited films are not fully dense and most likely have columnar structures. These columnar structures are detrimental for optical applications and to formation of barrier layers due to the scattering loss and pinholes caused by the structure. By applying a RF bias on wafer 16 during deposition, the deposited film can be densified by energetic ion bombardment and the columnar structure can be substantially eliminated.

[052] In the production of some embodiments of a barrier layer according to the present invention using, for example, the AKT-1600 based system, target 12 can have an active size of about 675.70 X 582.48 by 4 mm in order to deposit films on substrate 16 that can have dimension about 400 X 500 mm. The temperature of substrate 16 can be held at between about 50C and 500C. The distance between target 12 and substrate 16 can be between about 3 and about 9 cm. Process gas (for example, but not limited to, mixtures of Ar and O_2) can be inserted into the chamber

of apparatus 10 at a rate up to about 200 sccm while the pressure in the chamber of apparatus 10 can be held at between about 0.7 and 6 millitorr. Magnet 20 provides a magnetic field of strength between about 400 and about 600 Gauss directed in the plane of target 12 and is moved across target 12 at a rate of less than about 20-30 sec/scan. In some embodiments utilizing the AKT 1600 reactor, magnet 20 can be a race-track shaped magnet with dimension about 150 mm by 600 mm.

[053] Figure 1C shows a dielectric barrier layer 110 deposited on a substrate 120 according to the present invention. Substrate 120 can be any substrate, for example plastic, glass, Si-Wafers or other material. Substrate 120 may further include devices or structures that can be protected by barrier layer 110, such as organic light-emitting diode (OLED) structures, semiconductor structures, or other barrier layer structures. Barrier layer 110 can be a metallic oxide where the metal can be Al, Si, Ti, In, Sn or other metallic oxides, nitrides, halides, or other dielectrics. For example, a high index of refraction barrier layer can be formed by deposition of TiO_2 from a titanium target with example deposition parameters designated as 7KW/200W/200KHz/60Ar/90O2/950s (7 KW of pulsed-dc target power, 200 W of substrate bias power, 200 KHz is the pulsing frequency of the pulsed-dc target power, 60 sccm Ar gas flow, 90 sccm O_2 gas flow, 950s total deposition time). Another example lower index of refraction barrier layer can be formed from a target that is 92% Al and 8% Si (i.e. 92-8 or 92/8 layers) in a process designated as 3KW/200W/200KHZ/85Ar/90O2/1025 (3KW of pulsed-dc target power, 200 W of substrate bias power, 200 KHz pulsing frequency of the pulsed-dc target power, 85 sccm Ar flow, 90 sccm O_2 flow for 1025 sec of deposition time). As is further

discussed below, a wide range of process parameters can be utilized to deposit barrier layers according to the present invention.

[054] Barrier layers according to the present invention can be formed from any oxide materials. For example, MgO, Ta_2O_5, TiO_2, Ti_4O_7, Al_2O_3, SiO_2, silicon-rich SiO_2, and Y_2O_3. Oxide compounds of Nb, Ba, Sr, and Hf can also be utilized to form barrier layers according to the present invention. Further, barrier layers can be doped with rare-earth ions to produce optically active layers. Parameters provided herein for deposition of particular layers (e.g., the TiO_2 layers and the 92-8 layers discussed above) are exemplary only and are not intended to be limiting. Further, individual process parameters are approximations only. A wide range of individual parameters (e.g., power levels, frequencies, gas flows, and deposition times) around those stated can be used to form barrier layers according to the present invention.

[055] Dielectric barrier layer 110 can be characterized as a highly dense, uniform, defect free amorphous dielectric layer that may also have high optical transparency. Such films can be deposited in a pulsed-dc, substrate biased PVD process from a metallic target in an Ar/O_2 gas flow. As is further discussed below, some embodiments of dielectric barrier layer 110 have excellent surface roughness characteristics as well. Typically, as is discussed further below and with the examples and data provided, water vapor transmission rates for dielectric films according to embodiments of the present invention are tested in a MOCON test apparatus (MOCON referes to MOCON testing service of Minneapolis, MN) to be less than 1×10^{-2} $gm/m^2/day$ and are often less than 5×10^{-3} $gm/m^2/day$.

[056] Dielectric barrier stacks can be formed by depositing further barrier layers over barrier layer 110. Any number of stacked barrier layers can be utilized in order that the resulting structure not only function as a barrier layer, but may have other purposes in the resulting device as well. Further, a soft metallic breath treatment may be applied prior to deposition of a barrier layer according to embodiments of the present invention. A soft-metallic breath treatment refers to exposure of the substrate to a soft metallic vapor, as is further explained below.

[057] Figure 2A shows an embodiment of a dielectric stack 120 that can be utilized as a barrier structure as well as providing further optical functions. Dielectric stack 120 includes multiple barrier layers 101, 102, 103, 104, and 105 according to embodiments of the present invention. Each of barrier layers 101, 102, 103, 104, and 105 can be deposited utilizing deposition methods as described with more detail in U.S. Application Serial No. 10/101,863. The deposition is described generally above with respect to apparatus 10. In general, dielectric stack 120 can include any number of layers. In particular, dielectric stack 120 can include only a single barrier layer. The particular example of a barrier stack 120 shown in Figure 2A includes five layers, layers 101, 102, 103, 104 and 105. In the example of dielectric stack 120 shown in Figure 2A, dielectric layers 101, 103 and 105 are formed of a high index material such as titania (TiO_2). Layers 102 and 104 can be formed of a low index material such as silica (SiO_2), possibly doped with alumina (e.g., 92% silica and 8% alumina by cation percents, the 92-8 layer). Barrier stack 120 can be deposited directly on a substrate 100 as shown in Figure 2A or deposited on a layer 107 as shown in Figure 2D. Layer 107 is a layer to be protected from atmospheric contaminants or physical

damage and may include an optical or electrical device or another layer. Substrate 100 is a substrate on which layer 107 or dielectric stack 120 is formed. In some embodiments, substrate 100 can also provide a barrier to atmospheric contamination of layer 107. In some devices, further structures may be deposited over barrier layer structure 120.

[058] Table 1 illustrates deposition parameters for some example dielectric stack structures 120 according to the present invention. As described above, each of stacks 120 illustrated in Table 1 are formed utilizing an AKT 4300 PVD system using a Biased Pulsed DC Reactive Scanning Magnetron PVD Process as further described in U.S. Patent Application Serial No. 10/101,863, which has been previously incorporated by reference. Further, apparatus 10 as described above with respect to Figures 1A and 1B, can be clustered in the AKT 4300 PVD system with a loadlock chamber, an outgassing chamber, and may be equipped with plasma shields and a shield heater. As shown in Figure 2A, dielectric stack 120 for these examples includes 5 layers -- 3 alternating layers of TiO_2 and 2 layers of 92-8 SiO_2/Al_2O_3 (92%/8% by cation concentration).

[059] Dielectric stack 120 for each of the stacks shown in Table 1 was deposited directly on substrate 100. Substrate 100 for each of the stacks formed was first loaded into the loadlock of apparatus 10. The loadlock of apparatus 10 was pumped to a base pressure of less than about 10^{-5} Torr. The sheets of substrate 100, which may be of glass or plastic, was then transferred to a heat chamber of apparatus 10 and held at a temperature of about 300 °C for about 20 mins in order to outgas any moisture already accumulated by substrate 100. For polymer based substrates, for

example, the pre-heat step can be eliminated or performed at a lower temperature depending on the plastic substrate used. In some cases, the substrate and shield heaters of apparatus 10 can be disabled. The substrate column of Table 1 shows the composition of substrate 100 utilized in the deposition process.

[060] In each of stacks 1 through 6 illustrated in Table 1, the composition of the dielectric barrier layers in dielectric stack 120 is TiO_2/92-8/TiO_2/92-8/TiO_2, indicating that layers 101, 103 and 105 as shown in Figure 2A are TiO_2 layers and layers 102 and 104 as shown in Figure 2A are SiO_2/Al_2O_3 (92%/8% by cation concentration). The TiO_2 layers are deposited with the parameters shown in the TiO_2 Deposition Process column. The process details are given in the format: target power/bias power/pulsing frequency/Ar flow/O_2 flow/deposition time. Target power refers to the power supplied to target 12 of apparatus 10. Bias power refers to the power supplied by bias generator 18 to electrode 17 on which substrate 100 is mounted in place of substrate 16 as shown in Figure 1A and capacitively coupled to electrode 17. The Ar and O_2 flow rates across substrate 100 are then described in units of standard cubic centimeter/min (sccm). Finally, the deposition time is given. For example, the TiO_2 layers for stack number 1 illustrate in Table 1 were deposited with a target RF power of about 7 kW, with about 200 W of bias power, pulse frequency of about 200 KHz, an Ar flow rate of about 60 sccms, an O_2 flow rate of about 90 sccms, and a deposition time of about 950s. The measured thickness of a typical TiO_2 layer deposited according to the process described in the TiO_2 Deposition Process column is shown in the measured thickness TiO_2 column of Table 1.

[061] Similarly, the deposition parameters for deposition of silica/alumina layers for each dielectric stack 120 shown in Table 1 are shown in the silica/alumina (92/8) deposition process column. As indicated, each of the silica/alumina layers for stack numbers 1-6 shown in Table 1 are about 92% Silica and about 8% alumina by cation concentration. For example, in stack number 1 illustrated in Table 1, the silica/alumina layers were deposited with the power to target 12 being about 3 kW, the bias power to electrode 17 was about 200 W, the frequency of pulsed DC power supply 14 was about 200 kHz, the Ar flow rate was about 85 sccm, the O_2 flow rate was about 90 sccm, and the deposition time was about 1,005 sec.

[062] In general, in this disclosure a dielectric barrier layer referred to as 92/8 layer refers to a barrier layer formed from continuous deposition of a dielectric barrier layer from the 92% Silica/8% Alumina target. A dielectric barrier layer referred to as a 92-8 layer refers to a barrier layer formed in steps from the 92% Silica/8% Alumina target. A 92-8 layer can be formed, for example, on plastic substrates whereas 92/8 layers can be formed on Si-wafers or glass substrates that are not so sensitive to heat.

[063] In each of the stacks illustrated in Table 1, the reverse time for pulsed-DC power supply 14 was fixed at about 2.3 microseconds. The spacing between target 12 and substrate 100 was ~60mm, and the spacing between magnet 20 and target 12 was ~4-5 mm. The temperature of substrate 100 was about 200 °C and the shield heater of apparatus 10 was set to about 250 °C. The home offset of magnet 20 was set to be about 20 mm and the scan length was about 980 mm. The total pressure inside the chamber of apparatus 10, in plasma 53, during deposition of the

TiO_2 layers was about 5-6 mT. The total pressure inside the chamber, in plasma 53, during deposition of the silica/alumina layers was about 8-9 mT.

[064] In some barrier stacks according to the present invention, barrier layers are deposited by a reactively sputtered thin film layer or layers, formed by a process as previously described in the pulsed, biased deposition process, U.S. Application Serial No. 10/101,863. The pulsed, biased deposition process combines optical quality vacuum films having uniquely dense morphologies free of the columnar defects that are typical of non-biased vacuum thin films with parts per million uniformity and control of the optical index and birefringence. Very high resolution ellipsometry also demonstrates that a wide range of film index can be deposited with extinction coefficients which are zero across the visible and in the near IR region, and uniform on the order of parts per million providing substantially perfect transparency. As a result of the high level of densification and the low defect concentration, it is demonstrated that these very transparent films also provide superior diffusion barrier protection for moisture ingress as measured by steam permeation. Lastly, the same films demonstrate much higher dielectric breakdown under high voltage stress, also a result of the low levels of defects.

[065] Figure 8 shows a sample after exposure to a high-humidity, high temperature environment for an extended period of time. In the sample shown in Figure 8, about 200 nm of TiO_2 was deposited on a reactive aluminum layer that had been deposited on a 4" silicon wafer. The sample was kept in a chamber at about 85 °C with a relative humidity of about 100% for about 500 hours. As can be seen in

Figure 8, no defects are visible on the wafer indicating a high level of protection of the underlying reactive aluminum layer.

[066] Figure 9 shows a sample with a silica/alumina layer according to the present invention after exposure to a high-humidity, high-temperature environment for an extended period of time. In the sample shown in Figure 9, about 10 nm of aluminum is deposited on a 4" silicon wafer. About 100 nm of silica/alumina is deposited over the aluminum. The sample was then placed in a pressure cooker at about 250 °C with about 3.5 atm of saturated steam for about 160 hours. Again, no defects are visible on the wafer indicating a high level of protection of the underlying reactive aluminum layer. In another example, the thin reactive Al on a Si wafer was tested under the same conditions without a barrier layer and became transparent within minutes of the testing.

[067] Selected metal oxide films deposited with the previously disclosed process, from tens of nanometers to more than 15 microns, are not only impervious to moisture and chemical penetration as a film, but can also provide protection to an underlying layer or device from the effect of gas or moisture ingress while serving as an optical, electrical and/or tribological layer or device, rendering substantial manufacturing and environmental margins to the respective layers and devices. The subject process has been demonstrated on wide area substrates of glass and metal as well as low temperature material such as plastics.

[068] Table 4 shows Vickers Hardness (MPa) values obtained by testing an Al_2O_3 barrier layer and an Er-doped alumina/silicate (40% alumina/60% silica) films on a Si-Wafer. The Al_2O_3 barrier layer was deposited in a

3kW/100W/200KHz/30Ar/44O2/t process with a 2.2 μs reverse time. The Er, Yb doped Al_2O_3 was deposited with the process 6kW/100W/120KHz/60Ar/28O2/t process with a 1.2 μs reverse time. As can be seen in Table 4, the hardness as indicated generally by the Vickers number is large compared to conventionally deposited alumina films.

[069] Returning to Figure 2A, a dielectric stack 120 is deposited on substrate 100. Each of barrier layers 101, 102, 103, 104, and 105 can be optical layers (i.e., layers that are optically useful). Substrate 100 may be any glass, plastic, metallic, or semiconductor substrate. The thickness of layers 101, 102, 103, 104, and 105 of dielectric stack 120 can be varied to form either an anti-reflective coating or a reflective coating. Figure 2B shows a transparent conducting layer 106 deposited over dielectric stack 120. Transparent conducting layer 106 can be, for example, an indium tin-oxide layer. Figure 2C illustrates a substrate 100 with dielectric stacks 120 deposited on both a top surface and a bottom surface of substrate 100. The particular example shown in Figure 2C includes an embodiment of dielectric stack 120 with layers 101, 102, 103, 104, and 105 deposited on a top surface of substrate 100 and another embodiment of dielectric stack 120, shown having layers 108, 109, 110, 111, and 112 in Figure 2C, deposited on the bottom surface of substrate 100. Again, layers 108, 110, and 112 may be high index layers according to the present invention (e.g., TiO_2 layers) and layers 109 and 111 may be lower index layers such as silica/alumina layers. Examples of deposition parameters for dielectric stack 120 can be found in Table 1. As another example of a stack of barrier layers according to the present invention that provides good transmission characteristics is a four-layer stack

$TiO_2/SiO_2/TiO_2/SiO_2$ layering of thicknesses 12.43 nm, 36.35 nm, 116.87 nm, and 90.87 nm, respectively, deposited on glass provides a high transparency in the wavelength range of about 450 nm and 650 nm.

[070] In Figure 2D dielectric stack 120 is shown protecting a layer 107. Layer 107 is any layer of material that should be protected by a transparent barrier layer. For example, layer 107 may be a reactive metal such as aluminum, calcium or barium, layer 107 may be a fragile layer such as a conductive transparent oxide, or layer 107 may include an active optical or electrical device. As discussed above, the individual layers of dielectric stack 120 can provide protection both from incursion of atmospheric contaminants and protection against physical damage of layer 107. In some embodiments, the layer thickness of dielectric layers (e.g., layers 101, 102, 103, 104, and 105 shown in Figure 2D) of dielectric stack 120 are arranged to form either a transparent or reflective film at particular wavelengths. One skilled in the art can determine the thickness of individual films in dielectric stack 120 to form a reflective or anti-reflective film of dielectric stack 120. In some embodiments, where layer 107 is a metal such as aluminum, barium, or calcium, the device shown in Figure 2D forms a highly stable mirror. Figure 2E shows a dielectric stack 120 protecting a layer 107 where layer 107 has been deposited on substrate 100. Further, a transparent conducting layer 106 has further been deposited over dielectric stack 120. Figure 2F shows a structure where a second barrier stack 120 has been deposited on the bottom surface of substrate 100.

[071] Figure 10 shows a cross sectional SEM view of an example dielectric stack according to the present invention. Again, a five-layer TiO2/92-8 stack is

shown with thickness 550 nm for the TiO_2 layers and 970 nm for the 92-8 silica/alumina. The example shown in Figure 10 is a dielectric mirror stack such as that used to form a microcavity LED.

[072] Although Figures 2A through 2F show various configurations and utilizations of a barrier stack 120 having five layers, in general, a barrier stack 120 according to the present invention may be formed of any number of barrier layers. Further, the examples of barrier layers 101, 102, 103, 104, and 105 illustrated in Figures 2A through 2F illustrate examples of optical layers according to the present invention where those optical layers also function as self-protecting barrier layers in that they protect themselves as well as the particular surface or device on or below which they are deposited. Additionally, one or more of barrier layers 101, 102, 103, 104, and 105 may include optically active dopant ions such as rare-earth ions in order to provide more optically active functionality. Further, in accordance with the present invention, one or more of layers 101, 102, 103, 104, and 105 may be layers other than barrier layers according to the present invention. Each of the barrier layers described with respect to Figures 2A through 2F can be deposited utilizing a pulsed, biased deposition process as has been described in U.S. Application Serial No. 10/101,863 to form a highly densified layer of material with very low defect concentrations.

[073] Figure 3 shows another structure 321 utilizing dielectric stacks of barrier layers according to the present invention. As shown in Figure 3, structure 321 includes a dielectric stack 315 deposited on a substrate 316. Substrate 316 may be formed, for example, of glass or plastic materials. A transparent conductive layer 314, such as for example indium tin oxide, is deposited on dielectric stack 315. Layer

313 can be an electroluminescence layer such as, for example, a phosphor-doped oxide or fluoride material, rare earth doped silicon rich oxide light emitting device, or an organic light emitting polymer, OLED (organic light emitting diode) or polymer stack. A metal layer 312, which may be aluminum and may be doped with calcium or barium, is deposited on the side near layer 313. A second dielectric stack 317 can be formed on the bottom of substrate 316.

[074] Structure 321 illustrated in Figure 3 is an example of a microcavity enhanced LED, protected from water and reactive gas which may diffuse through substrate 316 by dielectric stacks 315 and 317. When layer 312 is a metal layer, a microcavity is formed between layer 312 and dielectric stack 315. Dielectric stack 315 can out-couple light emitted from electroluminescence layer 313. Layer 313 emits light when it is electrically biased as a result of a voltage applied between transparent conducting layer 314 operating as an anode and conducting layer 312 operating as a cathode. The layers of dielectric stack 315 and dielectric stack 317 may be arranged to contain the light emitted by layer 313 between layer 317 and metallic layer 312, forming an etalon arrangement to guide light along substrate 316. Additionally, dielectric layer 317 may be arranged to transmit light produced by layer 313, thereby forming a monitor arrangement with light being emitted substantially normal to substrate 316.

[075] Figure 11 illustrates the transmission data collected from examples of dielectric stacks according to the present invention. The metrology equipment utilized in taking the data resulting in Figure 11 was a Perkin Elmer Lambda-6 Spectrophotometer. Four samples were measured and each were 5 layer stacks of

TiO_2/92-8 as described above. Two samples have the same thickness layers (55 nm TiO_2 and 100 nm 92-8). As illustrated in Figure 11, the two different runs have almost the same transmission spectrum demonstrating the repeatability of the deposition process. The third example had a different thickness arranged so as to shift the transmission spectrum towards the blue. The fourth example was generated after the third example was maintained under 85/85 (85 C 85 % humidity) test conditions for 120 hours. It can be observed that the humidity and heat did not have a significant impact on the transmission characteristics of the mirror stack, again demonstrating the functionality of such dielectric stacks as protection layers as well as optical layers (i.e., no measurable wet-shift). A similar result was obtained after 500 hours of test with the 85/85 conditions with no measurable wet-shift.

[076] Figure 6 shows an example of another structure 633 with a microcavity enhanced LED structure 321 as described with Figure 3 covered and protected by a structure 622 such as those shown in Figures 2A through 2F. In structure 321, as shown in Figure 6, layers 314, 313, and 312 have been patterned. A structure 622 with dielectric stacks 618 and 620 deposited on opposite sides of a substrate 619 can be formed separately. Dielectric stacks 618 and 619 are formed as described with dielectric stacks 120 of Figures 2A through 2F. Structure 622 can then be epoxied over structure 321 in order to seal and protect structure 321. Epoxy layer 621, for example, can be an EVA epoxy.

[077] Figure 7 shows another structure 700 with an example of a microcavity enhanced LED structure 321 as described with Figure 3 covered and protected by a structure 623 such as those shown in Figures 2A through 2F. Covering

structure 623 includes substrate 619, with dielectric stack 620 deposited on substrate 619, epoxied to device 321.

[078] Figure 4 illustrates another example of barrier layers according to the present invention that also function as electrical layers (i.e., layers with electrical function such as providing resistance or function as the dielectric in a capacitor structure). The structure shown in Figure 4 illustrates an example of a bottom gate transistor structure 422 according to the present invention. Transistor structure 422 is formed on a substrate 416, which may be a plastic or glass material. In the embodiment illustrated in Figure 4, a dielectric stack 415 according to the present invention is deposited on a top surface of substrate 116 and a second dielectric stack 417 according to the present invention is deposited on a bottom surface of substrate 116. Dielectric stacks 417 and 415 each can include layers of high index and low index dielectric materials, as discussed above. The high index and low index dielectric materials, for example TiO_2 and silica/alumina layers as described above, each have low-voltage flat bands and low surface defects and therefore are suitable for use as thin film transistor structures. A semiconductor layer 423 is deposited on barrier stack 415 and patterned. Semiconductor layer 423 can be a semiconductor such as silicon, germanium, or may be of zinc oxide or a polymer material. Layers 424 and 425 form source and drain layers in contact with semiconductor layer 423. Layer 426 can be formed of a material with a high dielectric constant, such as any of the dielectric layers forming dielectric stacks 415 and 417, for example the high-dielectric strength TiO_2 material deposited by the processes described here. Layer 427 is an inter layer and layer 428 is the gate metal.

[079] Figure 5 shows an example of a top gate transistor device 529. Transistor device 529 is formed on a substrate 516 that is protected from atmospheric contamination (for example water or gasses) and physical wear and abrasion by dielectric stacks 515 and 517. Dielectric stacks 515 and 517 are formed from one or more layers of optical material as discussed above with dielectric stack 120. Gate layer 530 is deposited on dielectric stack 515. Layer 530 may be a metallic layer such as aluminum or chrome. A gate oxide layer 531 is deposited over layer 530. A semiconductor layer 532 is deposited on gate oxide layer 531 over layer 530. Semiconducting layer 532 can be similar to layer 423 of Figure 4. Layers 533 and 534 are source and drain layers, respectively, and are similar to layers 424 and 428 of device 422 of Figure 4 and may be formed from a conducting metal, conducting oxide, or a conducting polymer, for example.

[080] Dielectric stacks with barrier layers according to the present invention can have atomically smooth film surfaces, independent of the film thickness. Additionally, dielectric stacks with barrier layers according to the present invention can have film transparencies that are unmeasurably different from zero. These dielectric stacks represent a new capability for biased barrier film defect levels and barrier protection. Few products requiring dielectric barrier protection from water and oxygen, such as OLED displays, can tolerate a defect every square centimeter. Some embodiments of barrier layers as 2.5 nanometers and as thick as 15 microns have been deposited that exhibit an average surface roughness of about 0.2 nm, indicating a damage free process. Such layers exhibit an optical quality surface for all film thicknesses deposited, representative of the high amorphous film uniformity

attainable with these processes that produce embodiments of the barrier layer according to the present invention.

[081] Dielectric barrier layers according to the present invention have been shown to protect ultra thin reactive metal films of aluminum from steam heat oxidation from 125 to 250 °C at pressures of 3.5 ATM of pure steam for hundreds of hours with no visible defect on 100mm silicon wafers. Consequently, it is clear that both titanium oxide and alumina/silicate barrier layers, as described herein, can provide long term protection of reactive films which are pin hole free up to the area of one or both wafers. One pin hole in the protective dielectric barrier on a 100 mm wafer, with an area of approximately 75 square centimeters, would translate into a pin hole density of about 0.0133 per square centimeter. As shown in Figures 8 and 9, there were two wafers, one with aluminosilicate and one with titania barrier dielectric coatings, that were failure free. The total area between the two wafers was 150 square centimeters. If there were 1 defect on these two wafers the defect density would be 0.00666 per square centimeter. However, since the wafers were free of defects, the actual defect density could not be measured from the results of only two wafers. As indicated, then, the actual defect density was less than 0.0133 per square centimeter and likely less than 0.007 per square centimeter.

[082] In some embodiments of the invention, a soft metal, such as indium or indium-tin, breath treatment can be performed before deposition of one or more barrier layers such as those discussed above. It is likely that the soft metal breath treatment can be utilized to release stress between the dielectric barrier layer and the

substrate. Further, the soft metal breath treatment can act to nucleate for further growth of pin-hole free or defect-free barrier layer films on the substrate.

[083] Figures 12A and 12B show a single barrier layer structure 1200 with deposited on a substrate 1201 with and without a soft-metal breath treatment according to the present invention. In Figure 12A, a barrier layer 1203 such as is described above is deposited directly on substrate 1201. Substrate 1201 can be any suitable substrate material, including glass, plastic, or Si Wafers, for example. Substrate 1201 can, for example, include an OLED structure or other optically active structure which requires high optical throughput or an electrical structure that may utilize the barrier layers as electrical layers. Barrier layer 1203 can be any one or more barrier layers as is described above. As illustrated in Figure 12A, barrier layer 1203 can develop stress-related surface roughness during deposition and use.

[084] Figure 12B illustrates the results of depositing barrier layer 1203 following a soft-metal breath treatment according to some embodiments of the present invention. As is shown in Figure 12B, the stress is apparently relieved resulting in a barrier layer with much better surface smoothness.

[085] A soft-metal breath treatment according to some embodiments of the present invention includes an exposure of the substrate for a short time to a soft metal vapor followed by a heat treatment. An indium-tin breath treatment, for example, involves exposure of the substrate to indium-tin from an indium-tin target in a pulsed-dc process and a subsequent heat treatment. Direct exposure to indium-tin-oxide vapor does not yield the particular beneficial results illustrated below. Without being bound by a particular theory that may be presented in this disclosure, an In/Sn breath

treatment can relieve stress in the deposited barrier layer, improving surface smoothness and MOCON WVTR performance.

[086] In a particular example of formation of barrier layer structure 1200, an embodiment of a soft-metal breath treatment was performed on a plastic substrate 1201. A breath treatment of Indium/Tin, for example, can be performed from an Indium Tin (90%/10%) Target. The process for performing the indium/tin breath treatment can be designated as 750W/0W/200 KHz/20Ar/0O2/10sec. In other words, the pulsed-dc, biased, wide target PVD process is operated with a 90% Indium/10% Tin target, an Ar flow of 20 sccms running at a constant power of 750 W in a pulsed PVD system 10 (Figure 1A) (Pulsing Frequency 200 KHz, Reverse time 2.2 μsec) for 10 secs in the AKT 1600 PVD system using the Pinnacle Plus PDC power supply. Then, the breath treatment continued and substrate 1201 was transferred into a load lock of an AKT 4300 Tool and the Tool was pumped to a base pressure of less than about $1X10^{-5}$ Torr. The substrate was then transferred to a Heat Chamber at 130 °C at $1X10^{-8}$ Torr where it is thermally treated at 130 °C for about 25 min.

[087] Substrate 1201 (with the indium/tin breath treatment described above) was then moved to a second chamber where barrier layer 1203 is deposited. Barrier layer 1203 can be formed, as indicated above, from a 92-8 Alumino-Silicate (92% Si/8% Al) target with the deposition performed at room temperature.

[088] The process parameters for the deposition of the embodiment of 92-8 barrier layer 1203 can be 3KW/200W/200KHz/85Ar/90O2/x. Therefore, the process is performed with about 3 KW PDC power, about 200 KHz Pulsing Frequency, and about 2.2 microseconds reverse time. Bias power can be held at about 200 W. A Gas

flow of about 85 sccms of Ar and about 90 sccms of O_2 was utilized. In deposition of this particular embodiment, the deposition process was power cycled where the on cycle was about 180 secs long and the off cycle was about 600 secs long for 9 cycles. The thickness of the resulting barrier layer 1203 was then about 1600 Å. In a particular test, the process described above was utilized for deposition of a barrier structure 1200 with substrate 1201 being three plastic sheets of size 6 inch by 6 inch (Dupont Teijin PEN films 200 μm thick, referred to as a PEN substrate). In general, any barrier layer (e.g., the 92-8 or TiO_2 layers discussed above) can be deposited following a soft-metal breath treatment. As discussed before, examples of processes for embodiments of barrier layers according to the present invention are presented here but wide ranges of process parameters can result in barrier layers according to the present invention.

[089] Barrier layer structure 1200 on substrate 1201 can then be tested using a variety of techniques, some of which are described below. In particular, the stress in layer 1203 can be measured using a Flexus Stress Measurement technique. Surface roughness can be measured utilizing an atomic force microscope (AFM), and water vapor transmission rates (WVTR) can be measured in a high pressure, high humidity pressure cooker device.

[090] Figure 13 illustrates a Flexus Scanning Assembly 1300 that can be utilized to test barrier layer structure 1200. In Flexus Scanning Assembly 1300, a light beam for laser 1310 is directed onto the upper surface of barrier layer 1203 by a mirror 1312. The reflected light beam from barrier layer 1203 is detected by detector 1314. Detector 1314 measures the deflection of the light beam from the beam

reflected by mirror 1312. The optical section 1316, which can include laser 1310, mirror 1312, and detector 1314, can be scanned across substrate 1201 and the angle of deflection θ, which is related to the radius of curvature of substrate 1201 as shown in relation 1318.

[091] The thin film stress in barrier 1203 can be calculated utilizing the changes in substrate deformation measured by Flexus apparatus 1300 as optical portion 1316 is scanned. As is shown in relationship 1318, the angle of the reflected beam can be monitored during the scan and the inverse of the radius of curvature R of substrate 1201 can be calculated from the derivative of the angle as a function of position in the scan.

[092] In some cases, Flexus apparatus 1300 can utilize a dual wavelength technology to increase the range of film types that the tool is capable of measuring. Each Flexus apparatus 1300, then, can have more than one laser 1310 available for scanning the wafer since different film types will reflect different wavelengths of light. Further, the reflected laser intensity provides a good indication of the quality of the measurement. In general, low light intensity at detector 1314 indicates a poor measurement condition.

[093] In Flexus apparatus 1300, stress can be determined using Stoney's equation. In particular, stress in layer 1203 can be determined by measurements of the radius of curvature before deposition of layer 1203 and the radius of curvature after deposition of layer 1203. In particular, according to Stoney's equation, the stress can be given by

$$\sigma = \frac{E_s}{(1-\nu_s)} \frac{t_s^2}{6t_f} \left(\frac{1}{R_s} - \frac{1}{R_f} \right),$$

where $E_s/(1-\nu_s)$ is the biaxial modulus of substrate 1201, σ is the stress of substrate 1201, t_s is the substrate thickness, t_f is the film thickness, R_s is the pre-deposition radius of curvature, and R_f is the post deposition radius of curvature. To obtain the best results, both measurements of the radius of curvature should be performed on the same tool to minimize systematic error in the measured radius. In addition, because the shape of a wafer is unique and because stress is calculated based on the change in deformation of the substrate, each wafer should have a baseline radius measurement. A positive radius indicates tensile stress and a negative radius indicates compressive stress. Wafer bow can be calculated, as shown in Figure 14, by measuring the maximum point of deflection from the chord connecting the end-points of a scan of Flux apparatus 1300.

[094] Measurements of stress performed on several embodiments of barrier films 1203 where barrier film 1203 is a 92-8 film as discussed above with and without a nucleation layer 1202 formed by a soft-metal breath treatment is tabulated in Table 2. As shown in Table 2, sample 1 was a 1.5 KÅ 92-8 film of actual thickness 1760 Å deposited on a Si-Wafer substrate. The resulting stress at about room temperature was -446.2 MPa. Sample 2 was a 1.5 KÅ 92-8 film of actual thickness 1670 Å over an Al-breath deposition resulted in a stress of about -460.2 MPa. In sample 3, a 1.5 KÅ 92-8 film of thickness 1860 Å was deposited subsequent to a In-breath deposition and resulted in a stress of -330.2 MPa, nearly 100 MPa lower than either of the other two depositions depicted.

1, sample 2, and sample 3 as shown in Table 1 over a temperature cycle. The temperature cycle included heating from room temperature to about 160 °C and cooling back to room temperature. In a Si-Wafer substrate, the radius of the wafer is assumed not to change with temperature. Stress data in each case was taken at the temperature indicated. As can be seen from Figure 15, 92-8 films deposited over an In-breath treatment exhibited much less stress than did either a 92-8 film deposited over an Al-breath treatment or a 92-8 film deposited over the substrate without a soft-metal breath treatment.

[096] Atomic-force microscopy (AFM) can be utilized to measure surface roughness of a film. In AFM, a miniature probe is physically scanned over the surface of a film such that the probe is in contact, and follows the surface, of the film. The probe has a small tip and therefore is capable of accurately monitoring the surface roughness for features on the order of a few nanometers.

[097] Figure 16A shows the surface roughness of a PEN substrate (Dupont Teijin PEN films 200 μm thickness), before deposition of a barrier layer according to the present invention. As is shown in Figure 16A, a PEN substrate typically has a surface roughness of average 2.2 nm, root-mean-square average RMS of 3.6 nm, and a typical maximum roughness of about 41.0 nm. As shown in Figure 16B, deposition of a 1.5 KÅ 92-8 after an indium-tin breath treatment on a PEN substrate results in an average surface roughness of 1.0 nm with RMS roughness of 1.7 nm and maximum roughness of 23.6 nm. As is shown in Figure 16C, an indium-tin-oxide (ITO) breath treatment was performed before the 1.5 K Å 92-8 barrier layer film deposition

resulted in an average roughness of 2.1 nm with RMS roughness of 3.4 nm and maximum roughness of 55.4 nm. The deposition shown in Figure 16C is performed with a 125 μm PEN substrate rather than a 200 μm PEN substrate. Therefore, a direct ITO treatment does not perform as well as treatment with an indium-tin breath. As shown in Figure 16D, deposition of a barrier layer of 1.5 K Å directly on a 125 μm PEN substrate resulted in a barrier layer with average surface roughness of about 5.2 nm with RMS roughness of 8.5 nm and maximum roughness of 76.0 nm. Therefore, although the ITO breath treatment was better than no soft-metal treatment at all with respect to surface roughness, an indium-tin breath treatment resulted in the best surface roughness yielding an average surface roughness of about 1.0 nm.

[098] Figure 17 illustrates a water vapor transmission (WVTR) testing apparatus 1700 that can be utilized to characterize barrier layer films according to embodiments of the present invention. A sample 1701 can be mounted into apparatus 1700 in such a way that the surface of substrate 1201 (Figure 12) is isolated from the surface of barrier layer 1203 (Figure 12). A moisture-free gas is input to port 1702, contacts one surface of sample 1701, and is directed to sensor 1703 where the water vapor coming from sample 1701 is monitored. A humid gas is directed to the opposite side of sample 1701 through port 1705. An RH probe 1704 can be utilized to monitor the water content of the gas input to port 1705. Sensor 1703, then, monitors the water vapor that is transmitted through sample 1701.

[099] Such tests are performed by Mocon Testing Service, 7500 Boone Avenue North, Minneapolis, MN 55428. In addition, the Mocon testing is pereformed in accordance with ASTM F1249 standards. Typically, instruments

utilized for WVTR testing by Mocon can detect transmission in the range 0.00006gm/100in^2/day to 4gm/100in^2/day. The Mocon 3/31 instrument, for example, has a lower detection limit of about 0.0003gm/100in^2/day.

[0100] A barrier layer deposition formed with an Al-breath treatment followed by a 1.5 K Å 92-8 barrier layer deposition on a 200 μm PEN substrate resulted in a Mocon test WVTR of 0.0631 gm/100in^2/day. A barrier layer deposition formed with an In-breath treatment followed by a 1.5 K Å 92-8 on 200 μm PEN substrate resulting in no measurable WVTR in the Mocon 3/31 instrument (i.e., the transmission rate was less than 0.0003 gm/100in^2/day).

[0101] As was further discussed above, Figures 16A through D illustrates the role that a soft-metal breath treatment (in particular an indium breath treatment) can play in determining the surface roughness of a deposited barrier layer according to the present invention. The surface roughness of a barrier layer can also affect the WVTR characteristics of a barrier layer. Smoother barrier layer result in better WVTR performance. As such, Figure 16A shows a bare 200 μm PEN substrate with no barrier. Figure 16B shows a 200 μm PEN substrate with a 1500 Å thickness 92-8 barrier layer deposited after a In/Sn breath treatment according to the present invention. Figure 16C illustrates a 200 μm PEN substrate with a 1500 Å 92-8 barrier layer deposited after treatment with ITO breath. Figure 16D is a 200 μm PEN substrate with a 1500 Å 92-8 barrier layer directly deposited on the substrate. As can be seen, the structure of Figure 16B shows the best surface smoothness characteristics.

[0102] Table 3 illustrates several examples of barrier layers, with surface smoothness characteristics and MOCON WVTR testing results. In Table 3, the samples described in rows 1-4 are 92-8 layers (as described above) of thickness about 2000 Å deposited on one or both sides of a 700 μm thick polycarbonate (LEXAN produced by General Electric, corp.). The data shows that the double-side coated barrier layer structure (rows 1 and 2) perform about an order of magnitude better in MOCON WVTR test than does the one sided structures (rows 3 and 4).

[0103] Rows 5 through 8 illustrate various deposition on a PEN substrate (with rows 5-6 describing deposition on a 200 μm PEN substrate and rows 7 and 8 describing depositions on a 125 μm PEN substrate). The In breath treatment parameters refer to In/Sn breath treatments as discussed above. The AFM parameters are shown in Figures 16B through 16D as described earlier. As discussed before, the best surface smoothness and the best WVTR characteristics are shown in row 6, with In breath treatment followed by deposition of a 92-8 layer. The data in row 9 indicates an In breath treatment (In/Sn) with higher power on a thinner (125 μm) PEN substrate. Presumably, the thermal stress behavior on a 125 μm PEN substrate is worse than that for a 200 μm PEN substrate. Further indication of this effect is shown in the data of rows 30 through 33 along with Figures 19A and 19B. The data in rows 30 and 31 include a indium/tin breath treatment (at 750W) on a 200 μm PEN substrate followed by about 1.5 kÅ 92-8 layer deposition, which yields a very smooth surface (e.g., about 1.1nm average) as shown in Figure 19A and an undetectable MOCON WVTR characteristic on the MOCON 3/31 test equipment. The data in rows 32 and 33, with In/Sn breath treatment followed by 1.5 kÅ 92-8 layer deposition

on 125 μm PEN substrate, shows worse smoothness (about 2.0 nm average roughness) and a WVTR test in the MOCON apparatus of about 1.7 X 10^{-2} $gm/m^2/day$. The 92-8 depositions illustrated in rows 30 through 33 were concurrently performed in a single operation.

[0104] The data in rows 12 and 13 of Table 3 indicate an In-breath treatment plus 1.5 kÅ TiO_2 deposition on a 125 μm PEN substrate. Data in rows 10 and 11 indicate an In/Sn-breath treatment plus 1.5 kÅ 92-8 deposition on a 125 μm PEN substrate. As can be seen in Table 3, the WVTR characteristics of 92-8 layers is more than an order of magnitude better than the WVTR characteristics of TiO_2 layers. Representative smoothness for rows 12 and 13 are presented in Figure 22A and representative smoothness for rows 10 and 11 are presented in Figure 22B. As is shown in Table 3, the average smoothness for 92-8 layers is approximately an order of magnitude better than the average smoothness for TiO_2.

[0105] The data in rows 14 and 15 of Table 3 illustrate an In/Sn breath treatment on a 125 μm LEXAN substrate followed by a 92-8 layer deposition. The data in rows 14 and 15 can be compared with the data in rows 32 and 33, which are In/Sn breath treatment on a 125 μm PEN substrate followed by a 1.5 KÅ 92-8 layer deposition. The smoothness is comparable between the LEXAN and PEN substrate, although as can be seen in a comparison of Figures 21A and 21B, the morphology is different, i.e. barrier layers according to the present invention deposited on the LEXAN substrate show more granularity than barrier layers deposited on the PEN substrate.

[0106] The data in rows 16 through 18 of Table 3 illustrate different process parameters for an In/Sn breath treatment followed by 1.5 KÅ 92-8 deposition on a 200 μm PEN substrate. The data in row 16 illustrates a setting where the current is set rather than power. The data in row 16 is taken with a current of 6.15 amps. In the barrier layer illustrated in row 17, the In/Sn breath treatment is performed at 1.5 kW of operating power. In the barrier layer illustrated in row 18, the In/Sn breath treatment is performed at 750 W of operating power. In each case, the MOCON WVTR characteristic of the resulting barrier layer is below detectability on the MOCON 3/31 instrument.

[0107] The data in rows 19-29 of Table 3 illustrate different In/Sn breath treatments and their effects on the surface smoothness of the resulting barrier layers and on the MOCON WVTR characteristics. The data in rows 19-22 are all examples of where the In/Sn breath treatment is replaced with a evaporated In layer followed by a 130 C preheat treatment. The surface roughness characteristics are illustrated in Figure 18A and shows an average roughness of about 1.1 nm. However, the morphology is very granular as is shown in Figure 18A, with presumably a lot of porosity, resulting in MOCON WVTR test on the order of .8 $gm/m^2/day$. The data shown in row 23 of Table 3 illustrates the case where no In/Sn breath treatment is utilized and the 200 μm PEN substrate is preheated before deposition of a 1.5 kÅ 92-8 deposition, which as shown in Figure 18C has a surface roughness of about 5.2 nm average and a MOCON WVTR of about 0.8 $gm/m^2/day$, or the same as is shown with the indium evaporation vapor data shown in rows 19-22. Therefore, the same characteristics result whether an indium evaporation vapor treatment is applied or not.

[0108] Rows 24-29 of Table 3 illustrate data where an In/Sn breath treatment was performed at 280 °C rather than at room temperature. The surface roughness, as is illustrated in Figure 18B, was about 1.1 nm average. However, the MOCON WVTR data was about 3 X 10^{-2} gm/m^2/day. This value is much higher than that shown in the similar depositions of rows 30 and 31, which were below 5 X 10^{-3} gm/m^2/day detectability limits of the MOCON 3/31 instrument.

[0109] The data in rows 34 and 35 illustrates deposition of a 1.5 kÅ 35-65 layer (i.e., a deposition with a target having 35% Si and 65 % Al) following a In/Sn deposition on a 200 μm PEN substrate. As is illustrated, the MOCON WVTR are 1.4 X 10^{-1} gm/m^2/day, which shows the possible necessity of a biased process for producing barrier layers according to the present invention.

[0110] Figure 20 illustrates a barrier layer 2002 that can also operate as a thin film gate oxide deposited on a substrate 2001. A thin film gate oxide 2002 can be deposited as a barrier layer according to the present invention. Such a layer as the benefit of protecting moisture and oxygen sensitive transistor layer compounds of germanium, tin oxide, zinc oxide, or pentacene, for example, while functioning as the thin oxide electrical layer. Substrate 2001 can include any electrical device that can be formed on, for example, a silicon wafer, plastic sheet, glass plate, or other material. Barrier layer 2002 can be a thin layer, for example from 25 to 500 Å.

[0111] Titanium oxide is well known as the preferred material for biological implantation due to the lack of immunological response to titanium oxide. In addition, it is preferred that a thin film of TiO_2, which is an immunologically indifferent barrier layer, can simultaneously protect a device such as a voltage or

charge sensor or an optical device such as a waveguide while performing the role of coupling the device capacitively or optically due to its' high dielectric constant or its' high optical index.

[0112] An array of capacitors can be coupled by the high capacitive density due to the proximity of the sensor provided by a very thin high-k dielectric such as TiO_2. In practice, a micron or sub micron array can be used to monitor the electrical activity, amplitude, and direction of very low electrical signals such as those that accompany the propagation of electrical signals in single axion of single neural ganglia. Conversely, it can also be used to electrically couple stimulus to adjacent cells or tissue. High resolution, high-capacitance coupling to the optic nerve, the auditory nerve, or neural tissue on the order of 5 to 50 femto-farads/μm^2 is made uniquely feasible by such a capacitive barrier film without immunological reaction.

[0113] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. This disclosure is not limited by any theories or hypothesis of operation that are utilized to explain any results presented. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims. As such, this application is limited only by the following claims.

TABLE 1

Stack #	Substrates	Stack layer composition	TiO2 Deposition Process	Measured Thickness TiO2 (Å)	Silica/alumina (92-8) Deposition Process	Measured Thickness Silica/Alumina (92-8) (Å)
1	6 Microscope slides + 1 6inch wfr	TiO2/92-8/ TiO2/92-8/ TiO2	7KW/200W/200KHz/60Ar /90O2/950s	580	3KW/200W/200KHz/85Ar /90O2/1005	980
2	6 Microscope slides + 1 6inch wfr	TiO2/92-8/ TiO2/92-8/ TiO2	7KW/200W/200KHz/60Ar /90O2/835s	510	3KW/200W/200KHz/85Ar /90O2/1006	910
3	2 Sodalime Glass + 4 Microscope Slides	TiO2/92-8/ TiO2/92-8/ TiO2	7KW/200W/200KHz/60Ar /90O2/901s	550	3KW/200W/200KHz/85Ar /90O2/1025	1000
4	2 Sodalime Glass + 4 Microscope Slides	TiO2/92-8/ TiO2/92-8/ TiO2	7KW/200W/200KHz/60Ar /90O2/901s	550	3KW/200W/200KHz/85Ar /90O2/1025	1000
5	4 Microscope Slides	TiO2/92-8/ TiO2/92-8	7KW/200W/200KHz/60Ar /90O2/901s	550	3KW/200W/200KHz/85Ar /90O2/1025	1000
6	3 Sodalime Glass + 4 Microscope Slides	TiO2/92-8/ TiO2/92-8/ TiO2	7KW/200W/200KHz/60Ar /90O2/901s	550	3KW/200W/200KHz/85Ar /90O2/1025	1000

TABLE 2

Id	Comment	Temp °C	Radius (m)	Stress Mpa	Film Thickness (Å)	Bow (µm)
Sample 1	pre-deposition	21	-4.76E+03	N/A	N/A	1.58
	1.5 KÅ 92-8 film deposition/ no In-breath treatment	27	-145.978	-446.2	1760	11.74
Sample 2	pre-deposition	29	-4.10E+03	N/A	N/A	1.38
	Al breath deposition then 1.5 KÅ 92-8 film treatment	36	-169.482	-460.2	1670	10.18
Sample 3	pre-deposition	25	-230.249	N/A	N/A	4.36
	In breath treatment then 1.5 KÅ 92-8 film deposition	25	-67.169	-330.2	1860	10.25

TABLE 3

Sample ID	Sample Description	Substrate Material	Thickness µm	MOCON WVTR (g/100inch2/day)	MOCON WVTR (g/m2/day)	AFM Results
1 (Film (coated on both sides) - A)	2 KÅ 92-8 on Polycarbonate, deposited on both sides-A	LEXAN	700	7.2000E-04	1.1160E-02	
2 (Film (coated on both sides) - B)	2 KÅ 92-8 on Polycarbonate, deposited on both sides-B	LEXAN	700	5.8000E-04	8.9900E-03	
3 (Film (coated on one side) - A)	2 KÅ 92-8 on Polycarbonate - A	LEXAN	700	8.3000E-03	1.2865E-01	
4 (Film (coated on one side) - B)	2 KÅ 928 on Polycarbonate - B	LEXAN	700	1.7200E-02	2.6660E-01	
5 (Al+1.5K928)	Al -breath (500W 10sec+ 130c heat treatment) + 1.5 KÅ 92-8 on PEN	PEN Q65	200	6.3100E-02	9.7805E-01	

6 (InB + 1.5K928)	In Breath (750W 5sec+ 130c heat treatment) + 1.5 KÅ 92-8 on PEN	PEN Q65	200	3.0000E-04	4.6500E-03	Ra=1.3nm RMS=1.5nm Rmax=9.8nm *See* Figure 16B
7 (102-MOCON ID: 1619-003)	NO In Breath + 130c Preheat + 1.5 KÅ 92-8 on PEN	PEN Q65	125	4.0200E-02	6.2310E-01	Ra=5.2nm RMS=8.5nm Rmax=76.0nm *See* Figure 16D
8 (103-MOCON ID: 1619-002)	ITO breath + 130c Preheat + 1.5 KÅ 92-8 on PEN	PEN Q65	125	2.4900E-02	3.8595E-01	Ra=2.1nm RMS=3.4nm Rmax=55.5nm *See* Figure 16C
9 (104-MOCON ID: 1619-001)	In Breath (1.5KW + 130c Preheat) + 1.5 KÅ 92-8 on PEN	PEN Q65	125	2.5900E-02	4.0145E-01	
10 (PEN-A)	In Breath+92-8 on PEN	PEN Q65	125	1.8323E-03	2.8400E-02	Ra=3.4nm, RMS=4.2nm Rmax=29.4nm *See* Figure 22B
11 (PEN-B)	In Breath+92-8 on PEN	PEN Q65	125	2.3871E-03	3.7000E-02	Ra=3.4nm RMS=4.2nm Rmax=29.4nm *See* Figure 22B

12 (PEN2-A)	In Breath+TiO2 on PEN	PEN Q65	125	1.0065E-01	1.56	Ra=7.7nm RMS=9.7nm Rmax=72.4nm *See* Figure 22A
13 (PEN2-B)	In Breath+TiO2 on PEN	PEN Q65	125	8.9032E-02	1.38	Ra=7.7nm RMS=9.7nm Rmax=72.4nm *See* Figure 22A
14 (LEXAN-A)	InB+92-8 on LEXAN	LEXAN	125	1.4194E-02	2.2000E-01	Ra=0.9nm RMS=1.1nm Rmax=9.5nm *See* Figure 21A
15 (LEXAN-B)	In Breath+92-8 on LEXAN	LEXAN	125	2.8387E-03	4.4000E-02	Ra=0.9nm RMS=1.1nm Rmax=9.5nm *See* Figure 21A
16 (6.15A)	In Breath (6.15A 5sec+ 130 °C heat) + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	Below Detection	Below Detection	
17 (1.5KW)	In Breath (1.5KW 5sec+ 130 °C heat) + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	Below Detection	Below Detection	

18 (750W)	In Breath (750W 5sec+ 130 °C heat) + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	Below Detection	Below Detection	
19 (.037-A)	In Breath from Evap 0.037 + 130 °C Preheat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	5.1097E-02	7.9200E-01	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18A
20 (.037-B)	In Breath from Evap 0.037 + 130 °C Preheat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	3.9935E-02	6.1900E-01	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18A
21 (.113-A)	In Breath from Evap 0.113 + 130 °C Preheat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	5.6323E-02	8.7300E-01	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18A
22 (.113-B)	In Breath from Evap 0.113 + 130 °C Preheat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	4.1097E-02	6.3700E-01	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18A
23 (MON-A)	NO In Breath + 130 °C heat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	4.9806E-02	7.7200E-01	Ra=5.2nm RMS=8.5nm Rmax=76.0nm *See* Figure 18C

24 (12-17-03-01-A)	In Breath @280c+ 130 °C heat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	7.8710E-04	1.2200E-02	Ra=1.1nm, RMS=1.4nm Rmax=9.4nm *See* Figure 18B
25 (12-17-03-01-B)	In Breath @280c+ 130 °C heat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	1.1484E-03	1.7800E-02	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18B
26 (12-17-03-03-A)	In Breath @280c+ 130 °C heat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	1.9548E-03	3.0300E-02	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18B
27 (12-17-03-03-B)	In Breath @280c+ 130 °C heat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	1.1935E-03	1.8500E-02	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18B
28 (12-17-03-02_A)	In Breath @280c+ 130 °C heat + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#1	200	2.2065E-03	3.4200E-02	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18B
29 (12-17-03-02_B)	In Breath @280c+ 130 °C heat + 1.5 KÅ 92-8 on Pen	PEN Q65 Lot#1	200	2.7677E-03	4.2900E-02	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figure 18B

30 (165-A)	InB 750W 5sec+4300 130c Preheat + 1.5KA 92-8 on PEN	PEN Q65 Lot#2	200	Below Detection	Below Detection	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figures19A and 18D
31 (165-B)	In Breath (750W 5sec+130 °C heat) + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#2	200	Below Detection	Below Detection	Ra=1.1nm RMS=1.4nm Rmax=9.4nm *See* Figures 19A and 18D
32 (167-A)	In Breath (750W 5sec+ 130 °C heat) + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#2	125	9.0323E-04	1.4000E-02	Ra=2.0nm RMS=2.6nm Rmax=18.0nm *See* Figures 19B and 21B
33 (167-B)	In Breath (750W 5sec+ 130 °C heat) + 1.5 KÅ 92-8 on PEN	PEN Q65 Lot#2	125	1.4194E-03	2.2000E-02	Ra=2.0nm RMS=2.6nm Rmax=18.0nm *See* Figures 19B and 21B
34 (170-A)	In Breath (750W 5sec+130 °C heat) + 1.5 KÅ 35-65 (no bias) on PEN	PEN Q65 Lot#2	125	8.7742E-03	1.3600E-01	
35 (170-B)	In Breath (750W 5sec+130 °C heat) + 1.5 KÅ 35-65 (no Bias) on PEN	PEN Q65 Lot#2	125	2.6258E-02	4.0700E-01	

TABLE 4

	Hv [Vickers]	H [MPa]	E [GPa]	□ d [□m]
MN-Al2O3 5mN	1 836	19 814	211.49	0.129
MN-Al2O3 2.5mN	2 087	22 520	230.51	0.084
Y10822-1 5 mN	753	8 123	104.03	0.194
808-0Y10822-1 2.5 mN	834	8 996	104.29	0.130

WHAT IS CLAIMED IS:

1. A dielectric layer, comprising:

a densified amorphous dielectric layer deposited on a substrate by pulsed-DC, substrate biased physical vapor deposition,

wherein the densified amorphous dielectric layer is a barrier layer.

2. The layer of claim 1, wherein the deposition is performed with a wide area target.

3. The layer of claim 1, wherein the barrier layer is also an optical layer.

4. The layer of claim 3, wherein the barrier layer includes a TiO_2 layer.

5. The layer of claim 3, wherein the barrier layer includes an Alumina/Silica layer.

6. The layer of claim 3, further including a soft-metal breath treatment.

7. The layer of claim 6, wherein the soft-metal breath treatment is an indium-tin vapor treatment.

8. The layer of claim 1, wherein the barrier layer is also an electrical layer.

9. The layer of claim 8, wherein the barrier layer includes a capacitive layer.

10. The layer of claim 9, wherein the capacitive layer is a TiO_2 layer.

11. The layer of claim 9, wherein the capacitive layer is an Alumina/silica layer.

12. The layer of claim 8, wherein the barrier layer includes a resistive layer.

13. The layer of claim 12, wherein the resistive layer is indium-tin metal or oxide.

14 The layer of claim 8, further including a soft-metal breath treatment.

15. The layer of claim 14, wherein the soft-metal breath treatment is an indium-tin vapor treatment.

16. The layer of claim 1, wherein the barrier layer includes a tribological layer.

17. The layer of claim 16, wherein the tribological layer is a TiO_2 layer.

18. The layer of claim 16, wherein the tribological layer is Alumina/silica.

19. The layer of claim 16, further including a soft-metal breath treatment.

20. The layer of claim 19, wherein the soft-metal breath treatment is an indium-tin vapor treatment.

21. The layer of claim 1, wherein the barrier layer is a biologically immune compatible layer.

22. The layer of claim 1, wherein the biologically immune compatible layer is TiO_2.

23. The layer of claim 21, further including a soft-metal breath treatment.

24. The layer of claim 23 wherein the soft-metal breath treatment is an indium-tin vapor treatment.

25. The layer of claim 1, wherein the dielectric film is TiO_2.

26. The layer of claim 1, wherein a target utilized to form the dielectric film has a concentration of 92% Al and 8% Si.

27. The layer of claim 1, wherein the target utilized to form the dielectric film is formed from metallic magnesium.

28 The layer of claim 1, wherein the target material comprises materials chosen from a group consisting of Mg, Ta, Ti, Al, Y, Zr, Si, Hf, Ba, Sr, Nb, and combinations thereof.

29 The layer of claim 28, wherein the target material includes a concentration of rare earth metal.

30 The layer of claim 1, wherein the target material comprises a sub-oxide of a group consisting of Mg, Ta, Ti, Al, Y, Zr, Si, Hf, Ba, Sr, Nb, and combinations thereof.

31. The layer of claim 1, further including a soft-metal breath treatment.

32. The layer of claim 31, wherein the soft-metal breath treatment is an indium-tin vapor treatment.

33. The layer of claim 1, wherein the dielectric film has a permeable defect concentration of less than about 1 per square centimeter.

34. The layer of claim 1, wherein the water vapor transmission rate is less than about 1 X 10^{-2} gm/m^2/day.

35. The layer of claim 1, wherein the optical attenuation is less than about 0.1 dB/cm in a continuous film.

36. The layer of claim 1, wherein the barrier layer has a thickness less than about 500 nm.

37. The layer of claim 36, wherein the water vapor transmission rate is less than about 1 X 10^{-2} gm/m^2/day.

38. The layer of claim 1, wherein the barrier layer thickness is less than about 1 micron and the water vapor transmission rate is less than about 1 X 10^{-2} gm/m^2/day.

39. The layer of claim 1, wherein the barrier layer operates as a gate oxide for a thin film transistor.

40. A method of forming a barrier layer, comprising:

providing a substrate;

depositing a highly densified, amorphous, dielectric material over the substrate in a pulsed-DC, biased, wide target physical vapor deposition process.

41. The method of claim 40, further including

performing a soft-metal breath treatment on the substrate.

42. The method of claim 40, wherein the dielectric material is formed from a target comprising 92% Al and 8% Si.

43. The method of claim 40, wherein the dielectric material is formed from a target comprising of Titanium.

44. The method of claim 40, wherein the dielectric material is formed from a target material comprising materials chosen from a group consisting of Mg, Ta, Ti, Al, Y, Zr, Si, Hf, Ba, Sr, Nb, and combinations thereof.

45. The method of claim 41, wherein the soft-metal breath treatment is an indium/tin breath treatment.

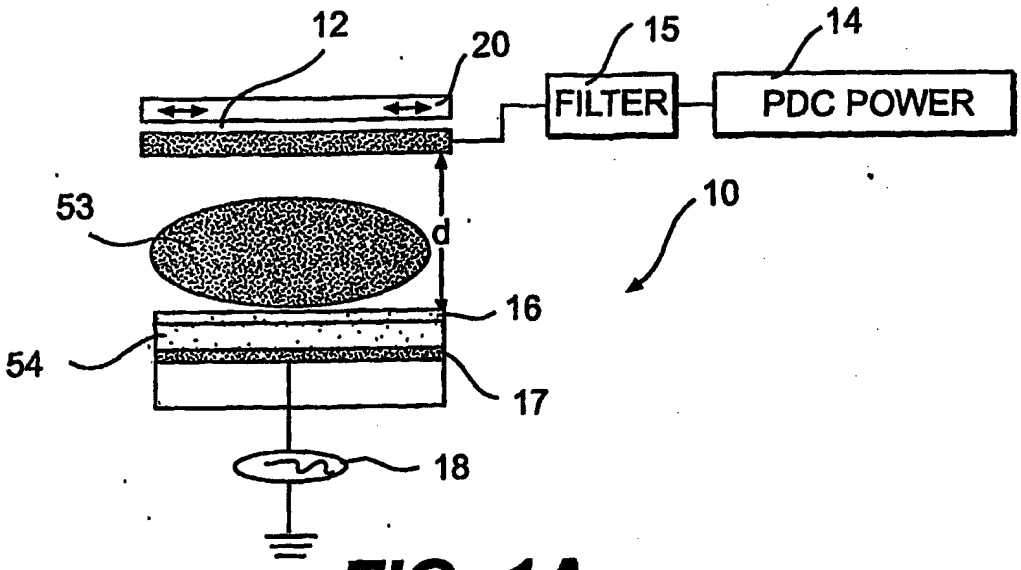


FIG. 1A

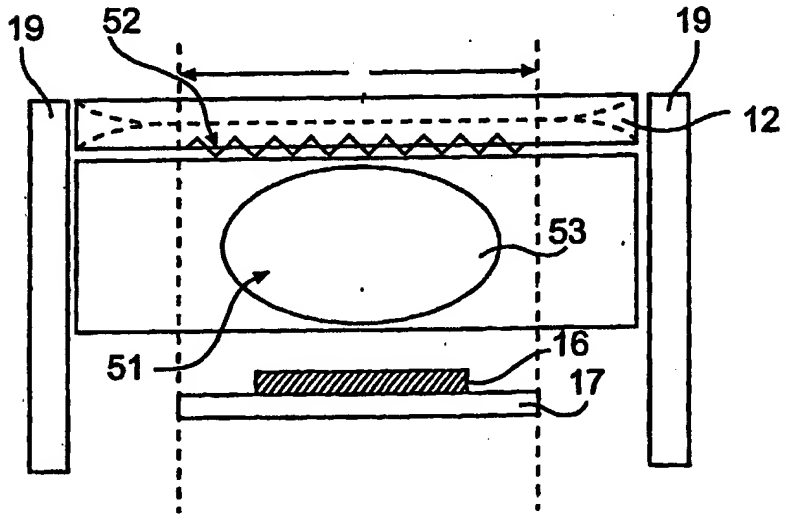


FIG. 1B

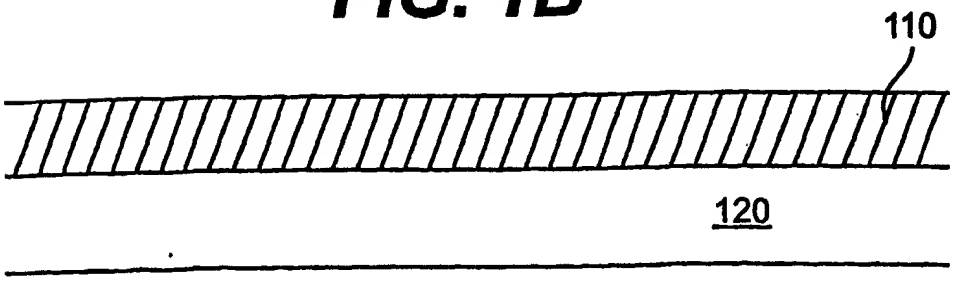


FIG. 1C

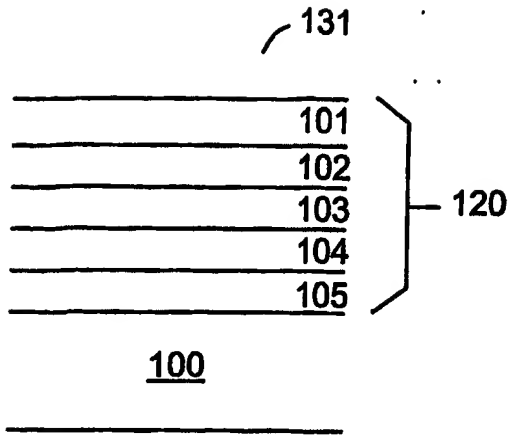


FIG. 2A

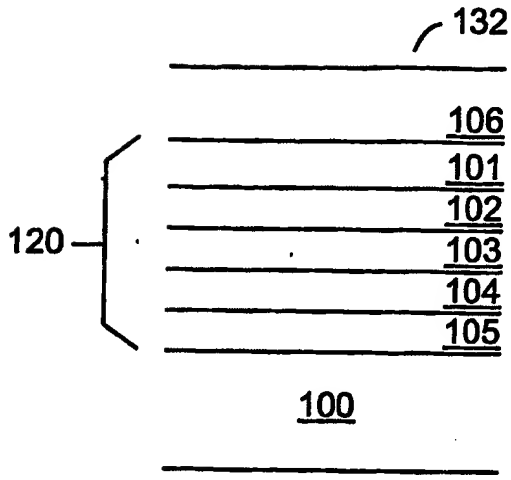


FIG. 2B

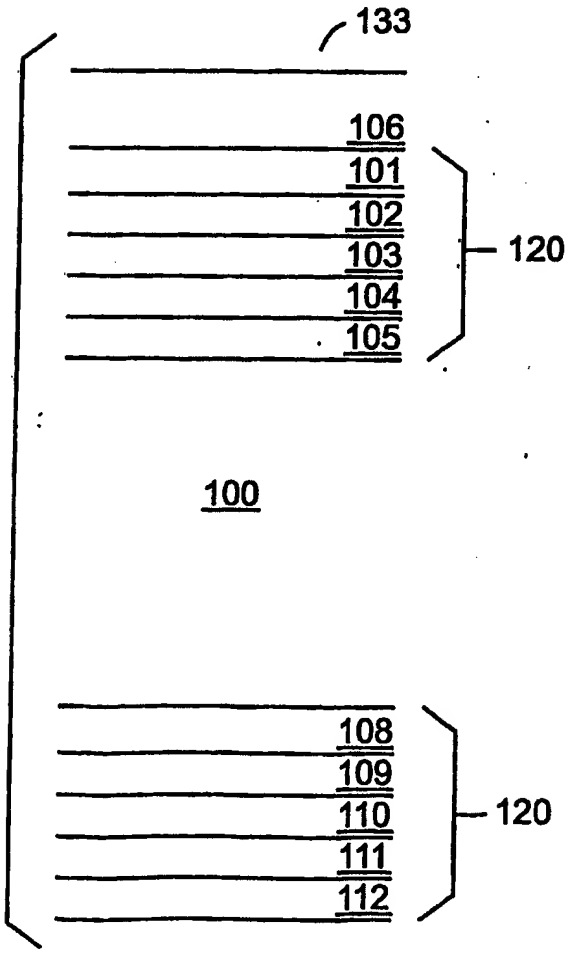


FIG. 2C

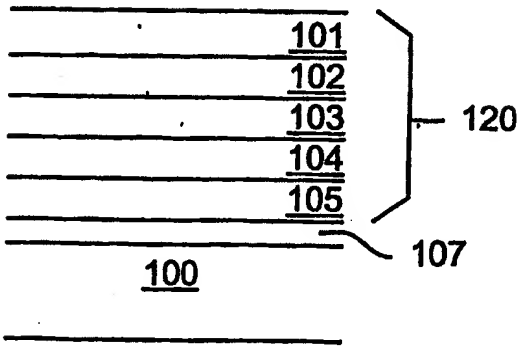


FIG. 2D

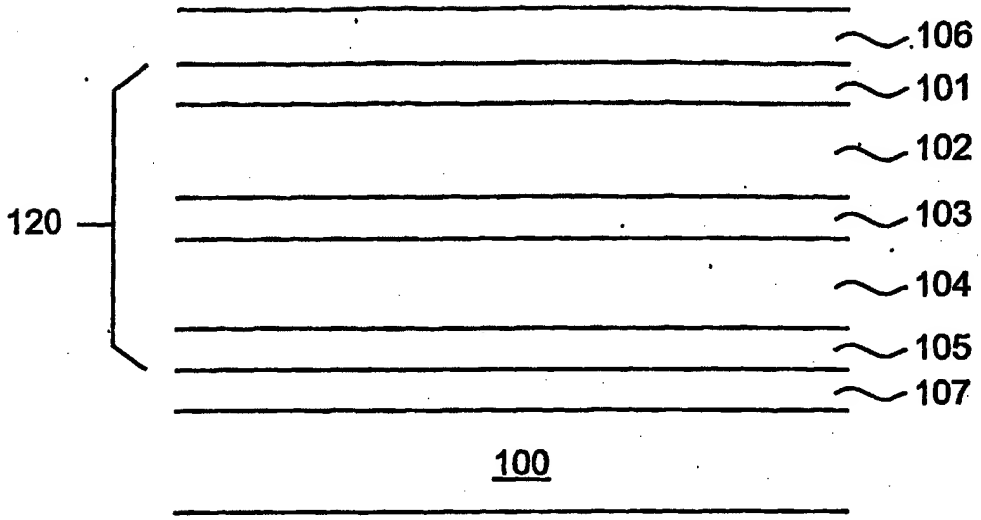

106
101
102
120
103
104
105
107
100

FIG. 2E

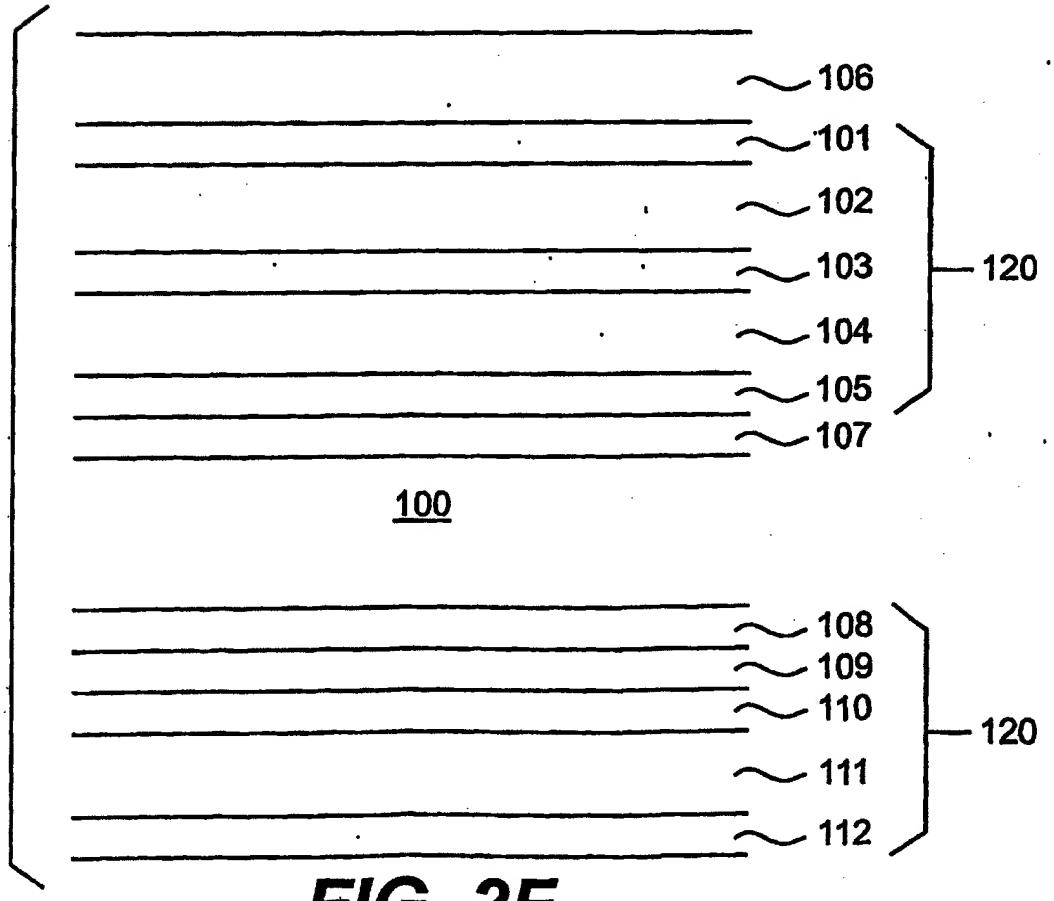

106
101
102
103
120
104
105
107
100
108
109
110
120
111
112

FIG. 2F

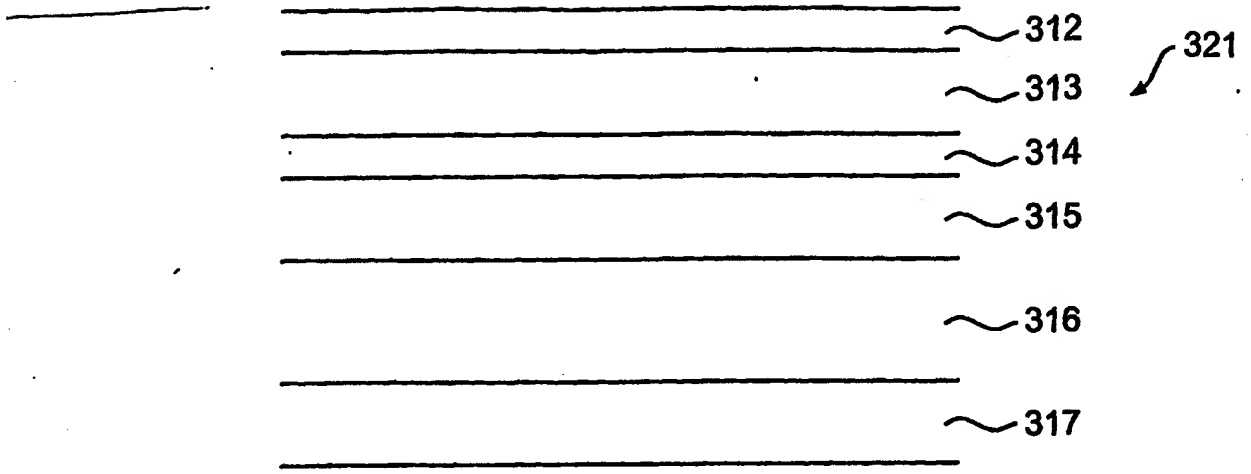


FIG. 3

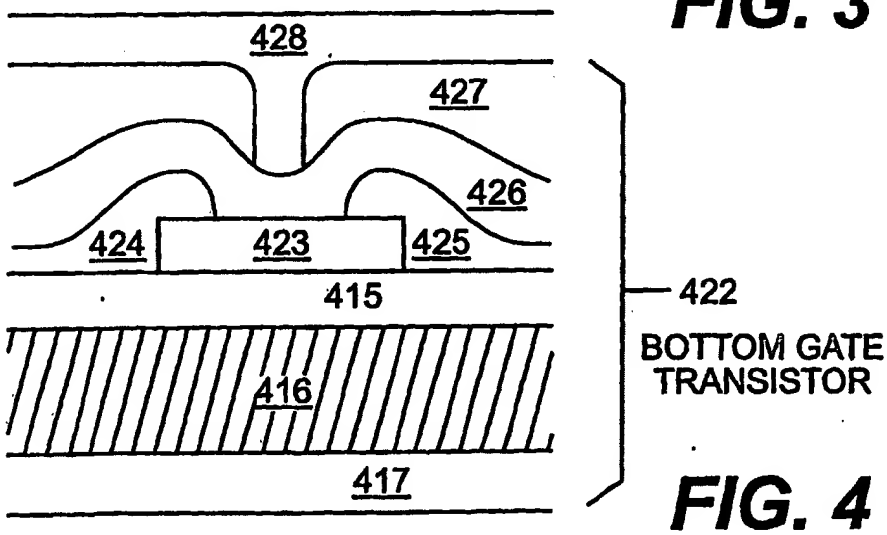


FIG. 4

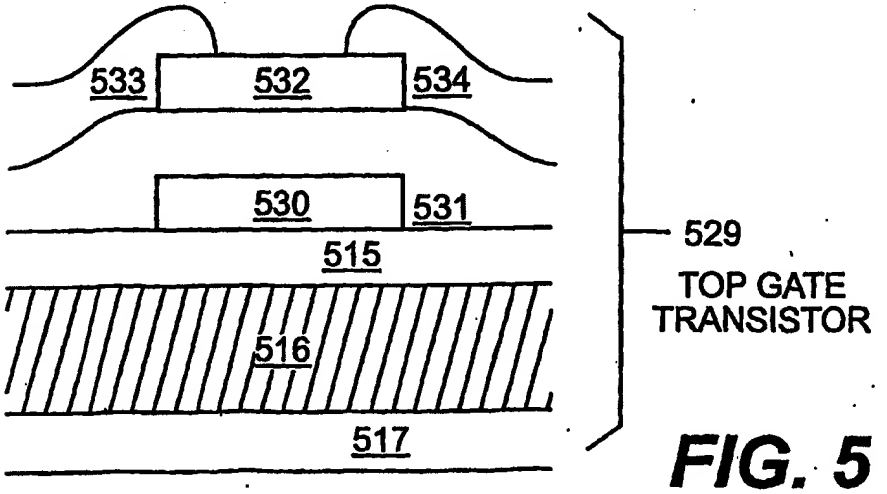


FIG. 5

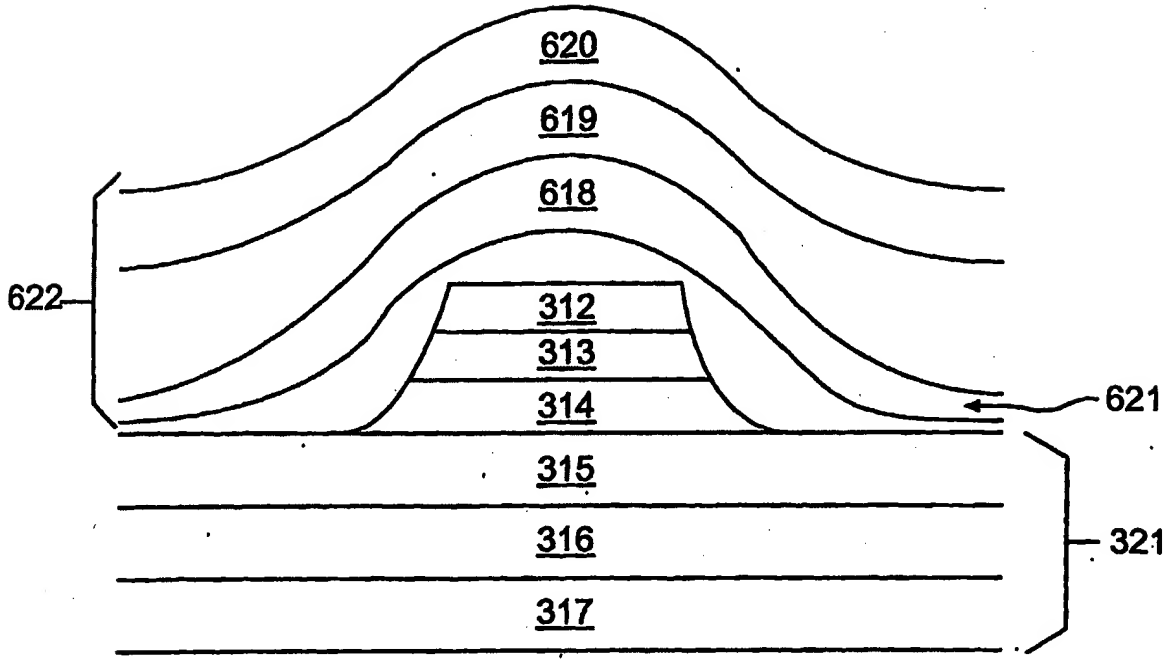

620
619
618
622
312
313
314
621
315
316
321
317

FIG. 6

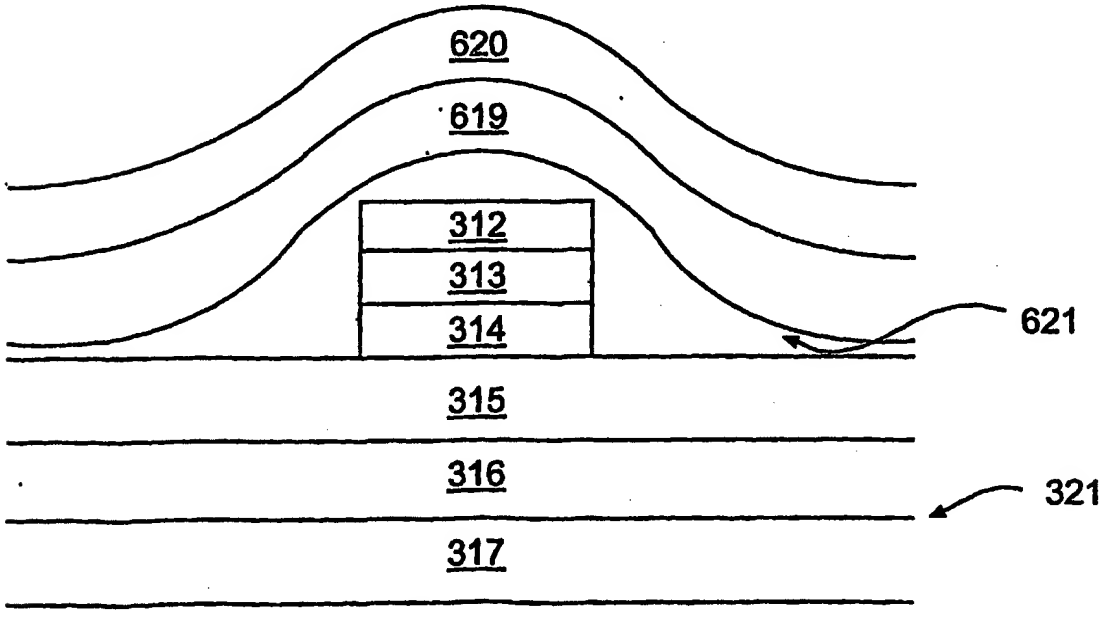

620
619
312
313
314
621
315
316
321
317

FIG. 7

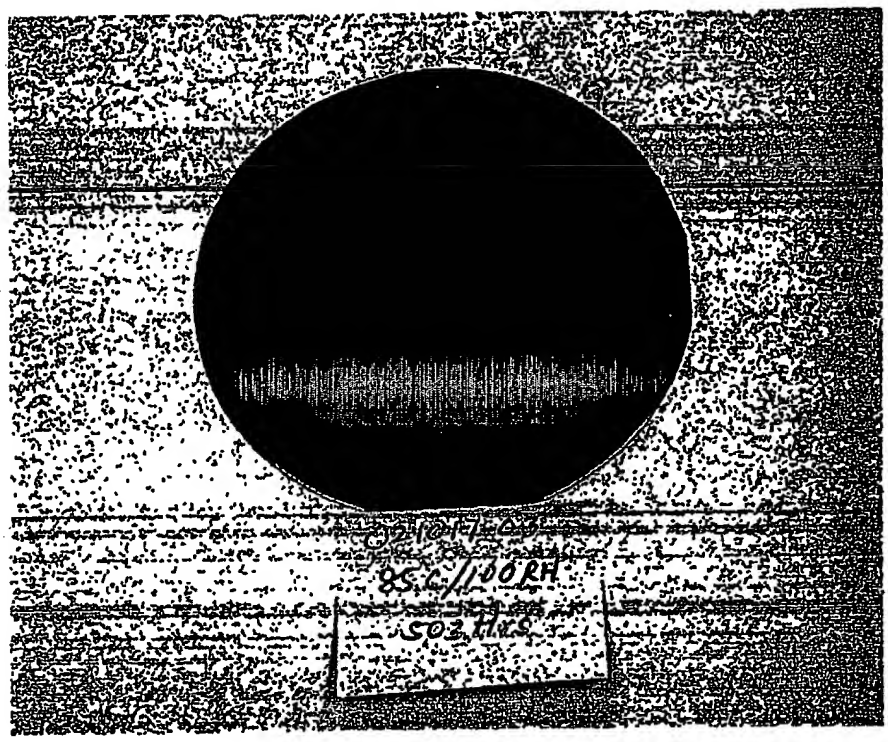


FIG. 8

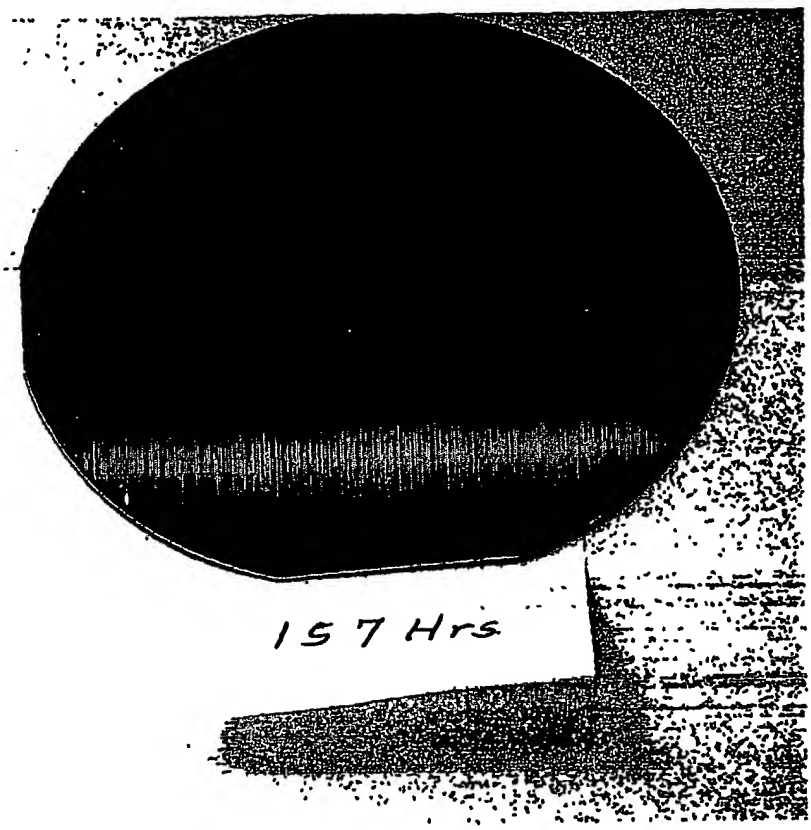
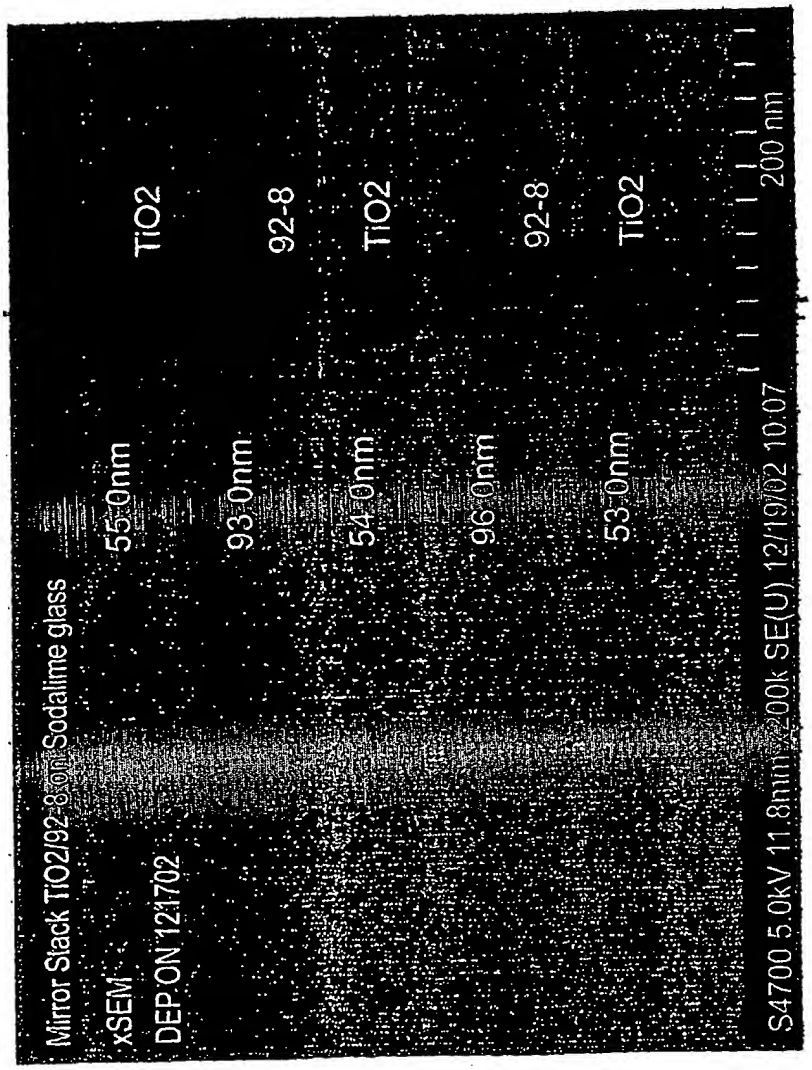


FIG. 9

FIG. 10


Mirror Stack TiO2/92-8 on Sodalime glass
xSEM
DEP ON 121702
55.0nm
TiO2
93.0nm
92-8
54.0nm
TiO2
96.0nm
92-8
53.0nm
TiO2
200 nm
S4700 5.0kV 11.8mm x200k SE(U) 12/19/02 10:07

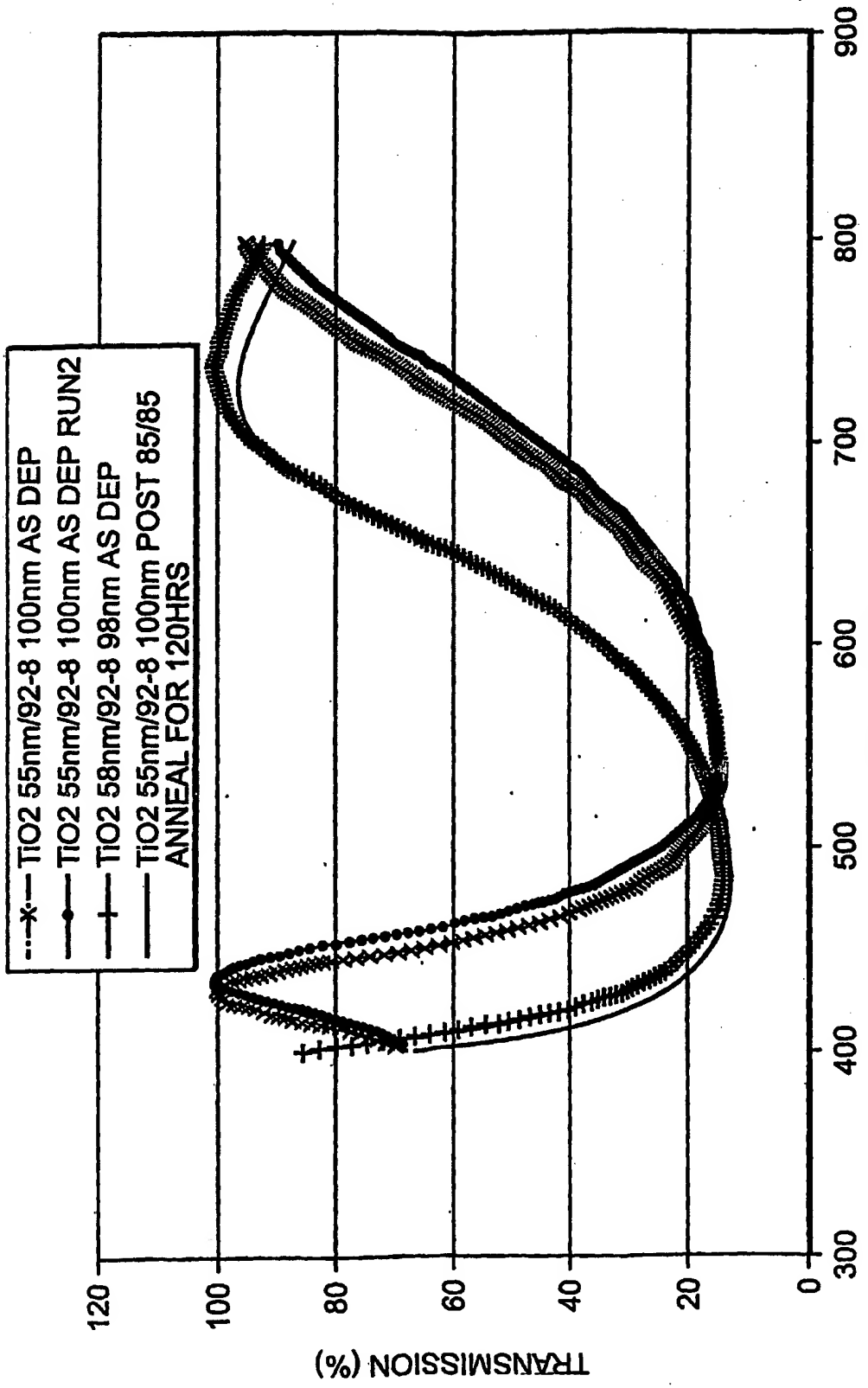

TiO2 55nm/92-8 100nm AS DEP
TiO2 55nm/92-8 100nm AS DEP RUN2
TiO2 58nm/92-8 98nm AS DEP
TiO2 55nm/92-8 100nm POST 85/85 ANNEAL FOR 120HRS
120
100
80
60
40
20
0
TRANSMISSION (%)
300
400
500
600
700
800
900
WAVELENGTH (nm)

FIG. 11

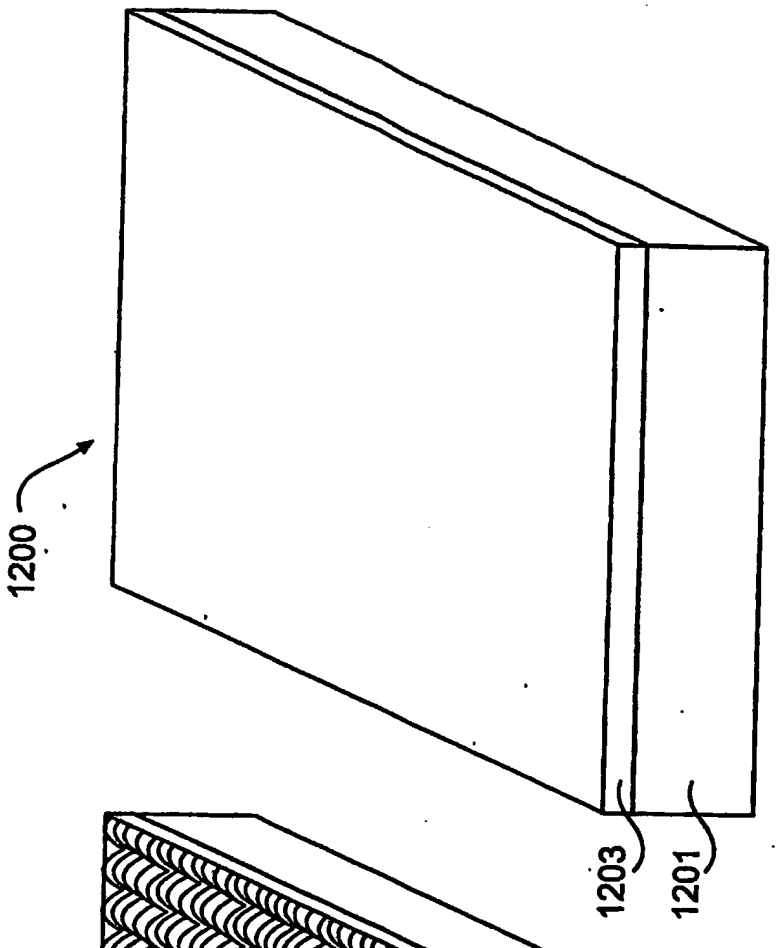


FIG. 12B

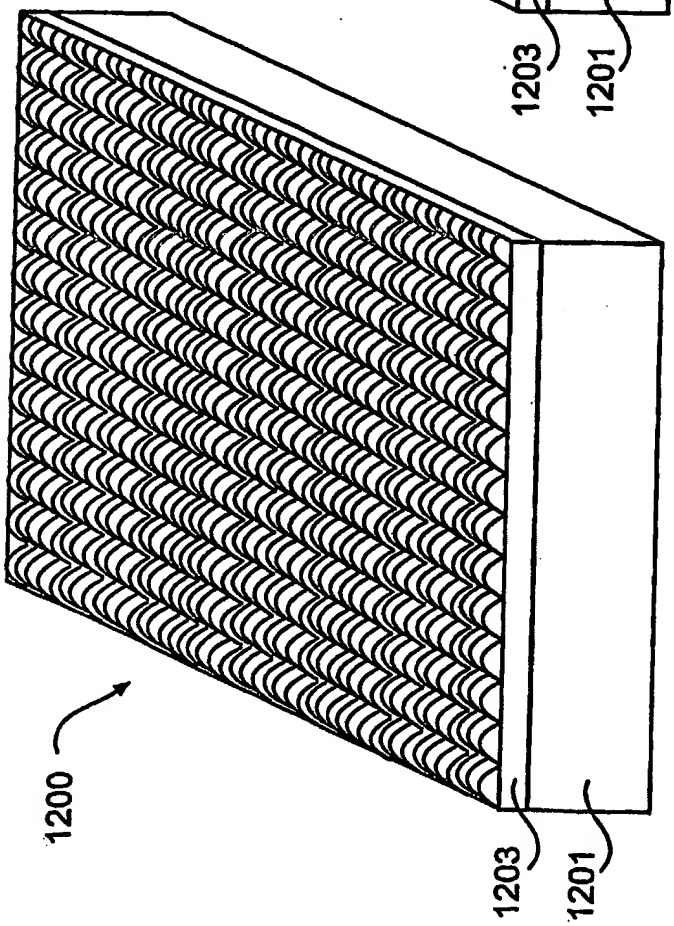


FIG. 12A

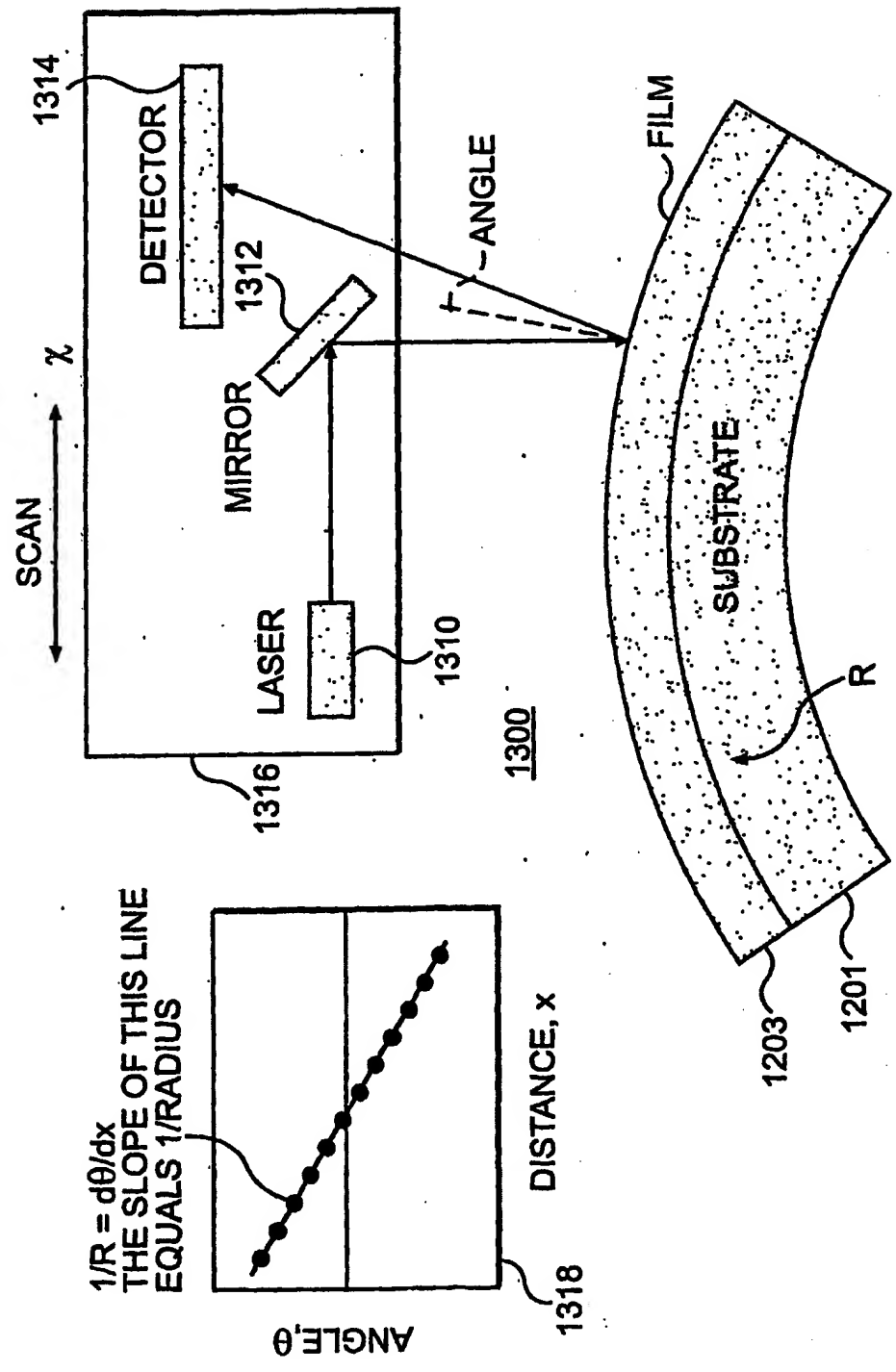

1314
DETECTOR
1312
MIRROR
LASER
1310
SCAN
χ
1316
1300
ANGLE
FILM
SUBSTRATE
R
1203
1201
1/R = dθ/dx
THE SLOPE OF THIS LINE
EQUALS 1/RADIUS
DISTANCE, x
ANGLE, θ
1318

FIG. 13

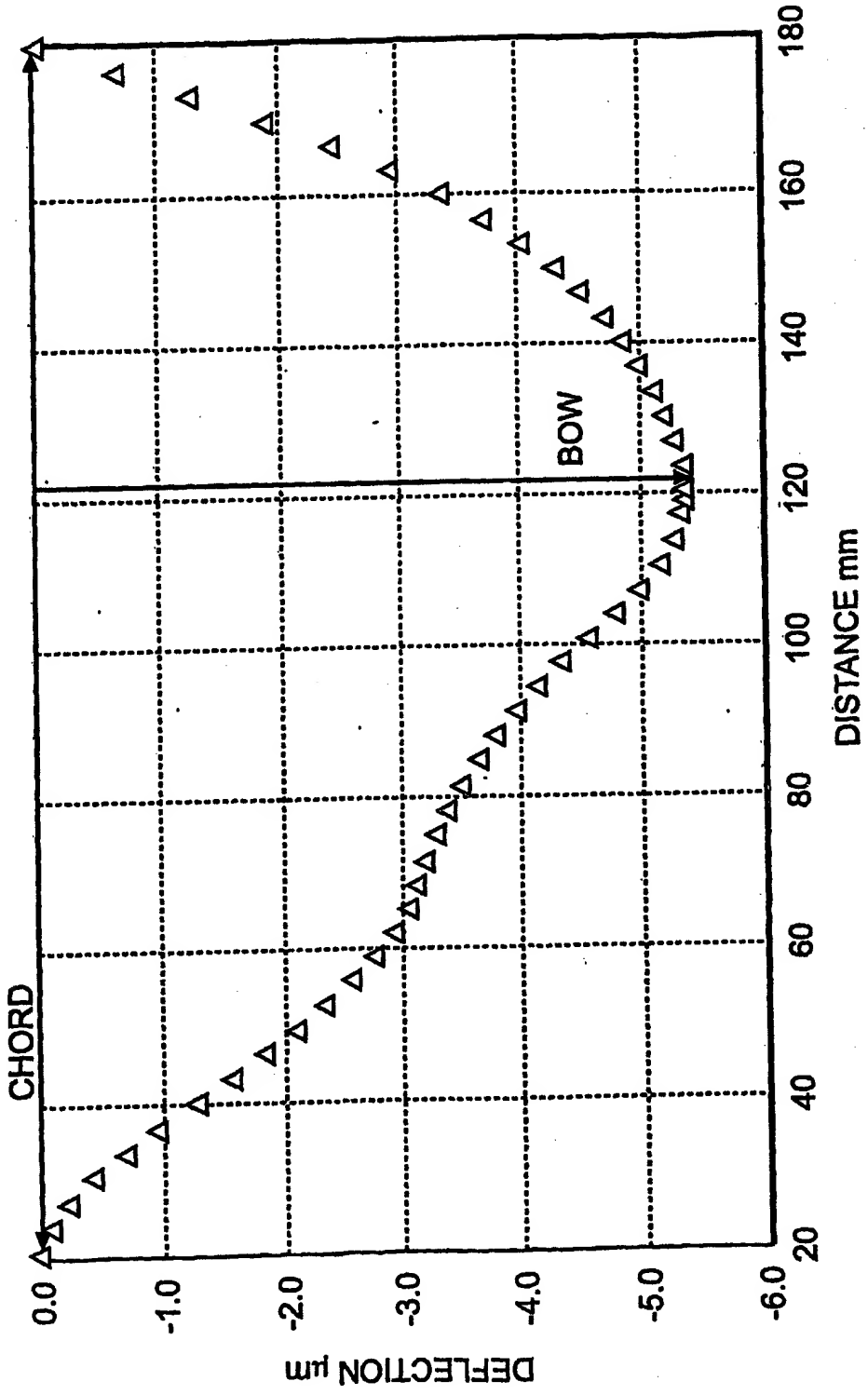

CHORD
BOW
DISTANCE mm
DEFLECTION μm
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
-6.0
20
40
60
80
100
120
140
160
180

FIG. 14

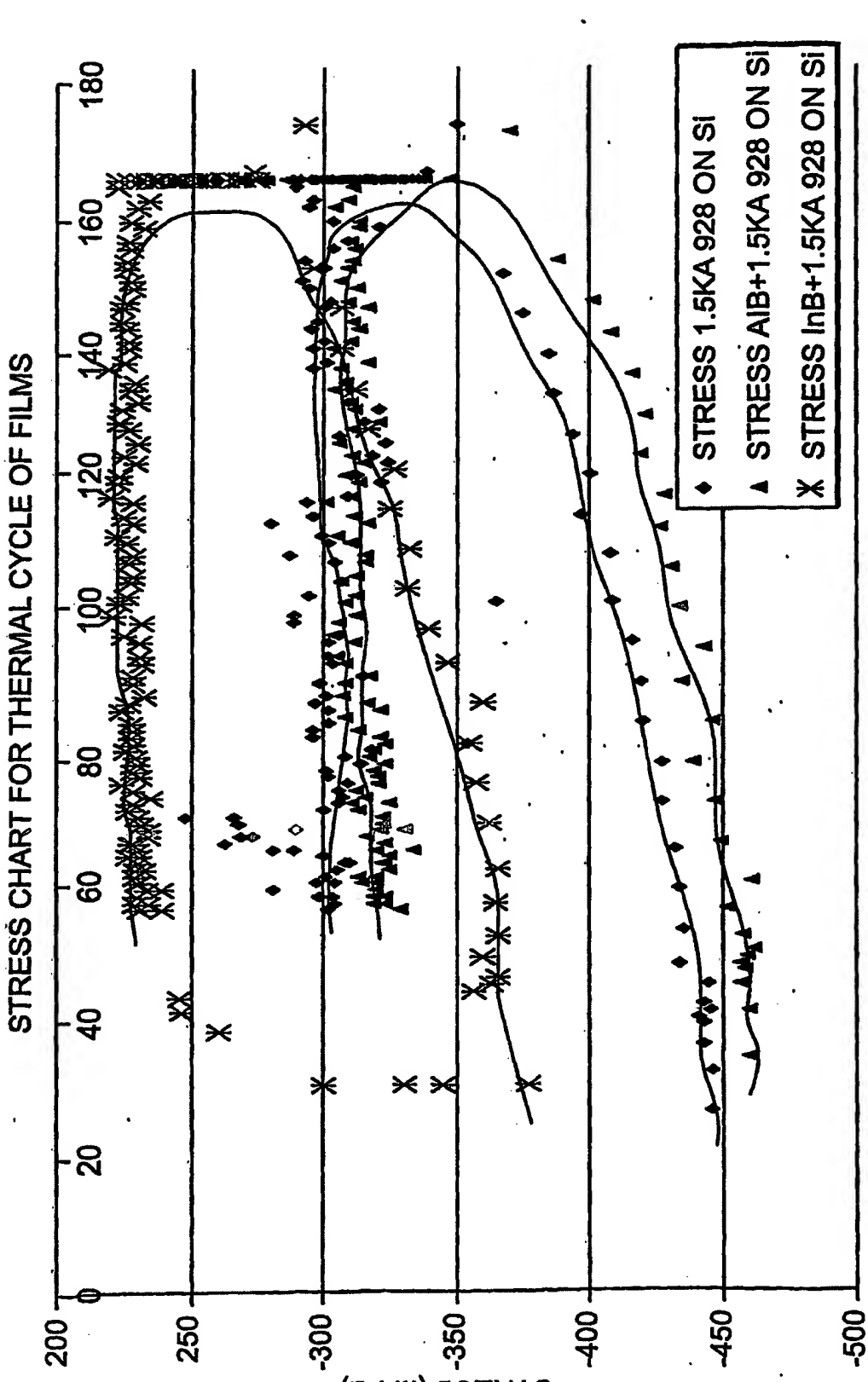

STRESS CHART FOR THERMAL CYCLE OF FILMS
STRESS 1.5KA 928 ON Si
STRESS AlB+1.5KA 928 ON Si
STRESS InB+1.5KA 928 ON Si
TEMPERATURE (C)
STRESS (M Pa)
0
20
40
60
80
100
120
140
160
180
200
250
-300
-350
-400
-450
-500

FIG. 15

FIG. 16B

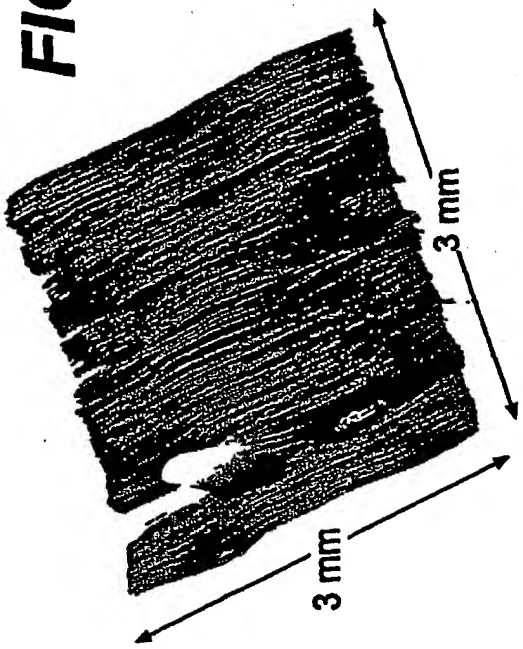


FIG. 16D

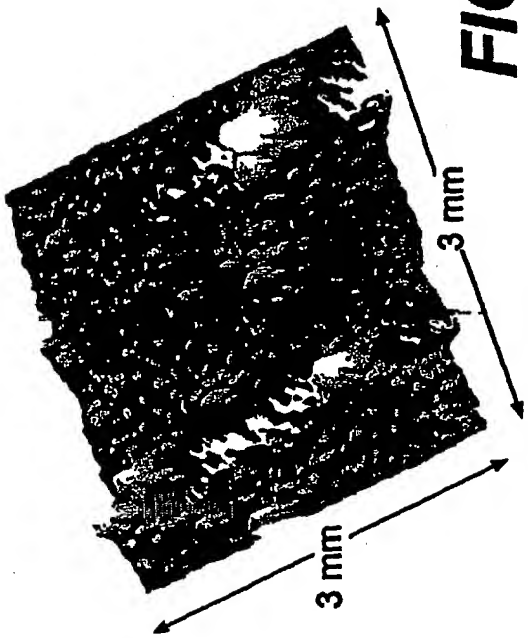


FIG. 16A

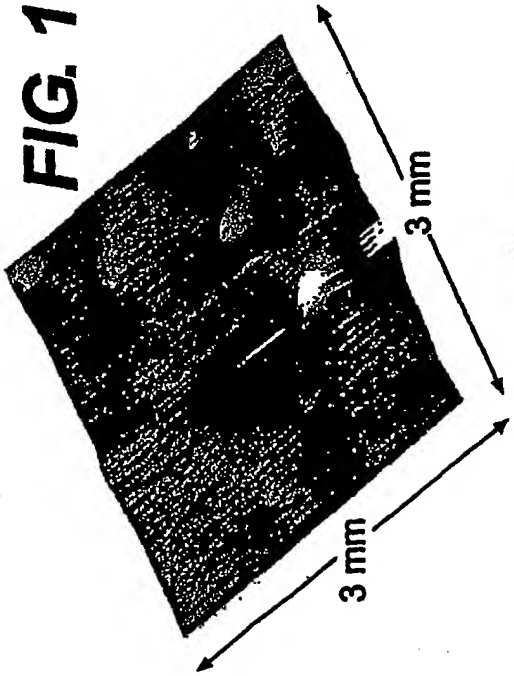
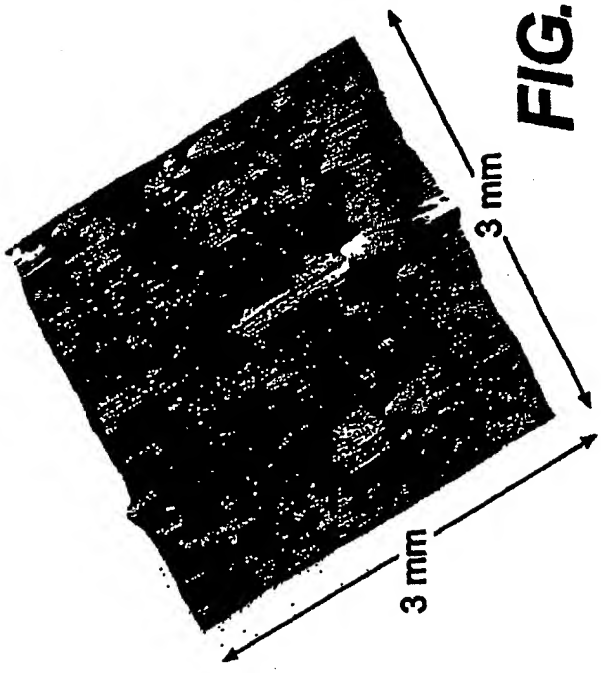


FIG. 16C



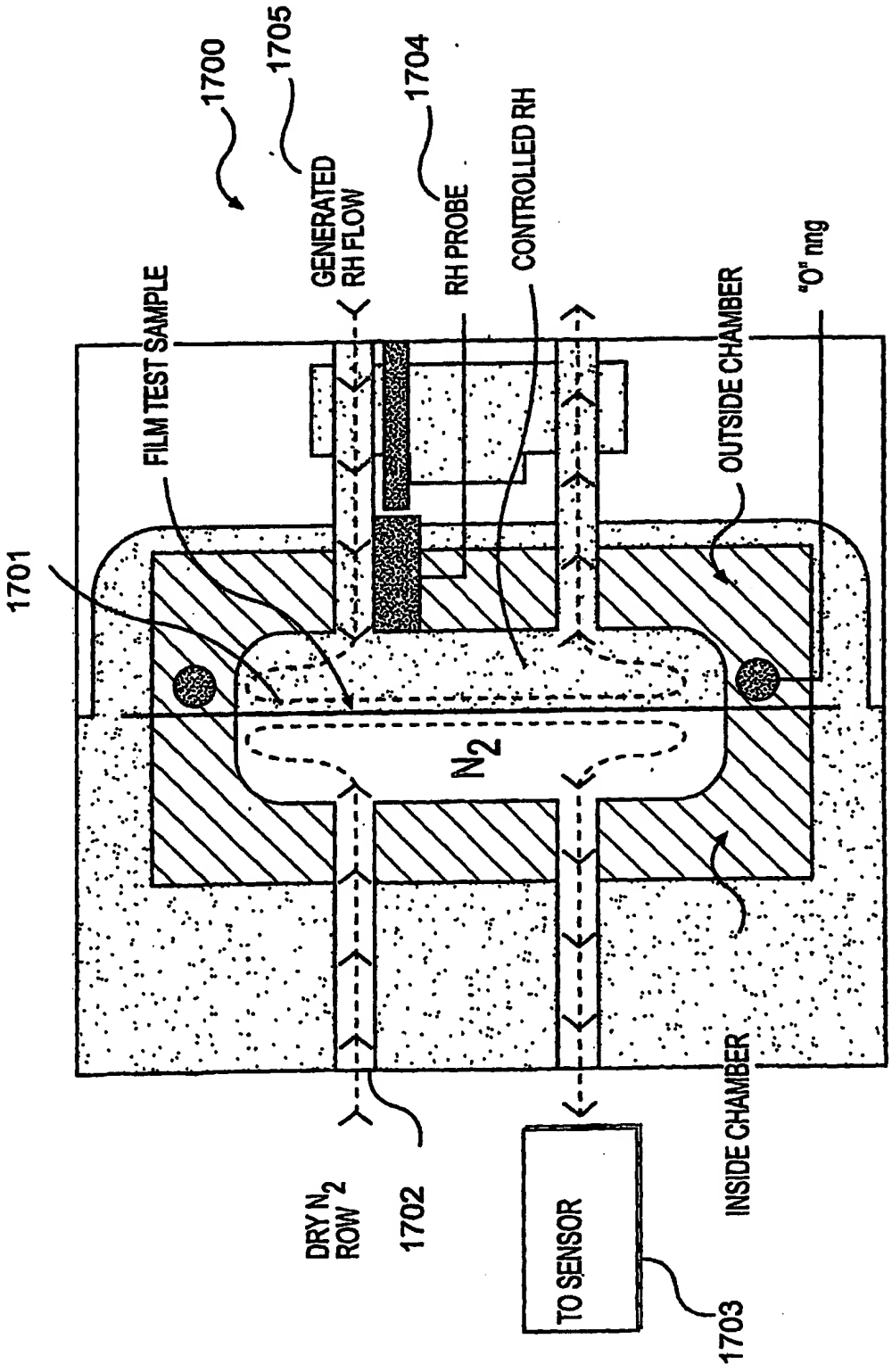

1700
1705
1704
GENERATED RH FLOW
RH PROBE
CONTROLLED RH
FILM TEST SAMPLE
OUTSIDE CHAMBER
"0" mg
1701
N_2
DRY N_2 ROW
1702
TO SENSOR
INSIDE CHAMBER
1703

FIG. 17

FIG. 18B

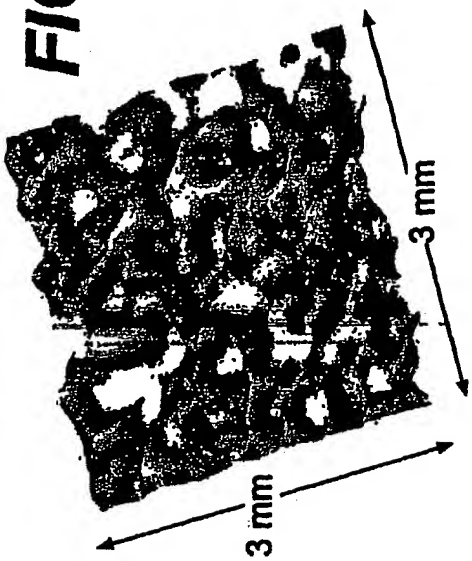


FIG. 18D

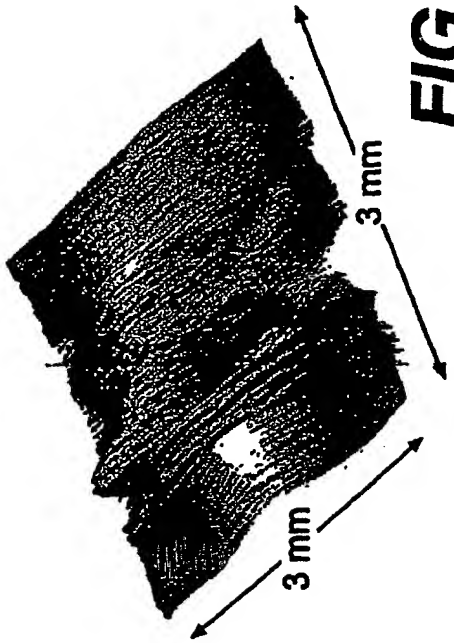


FIG. 18A

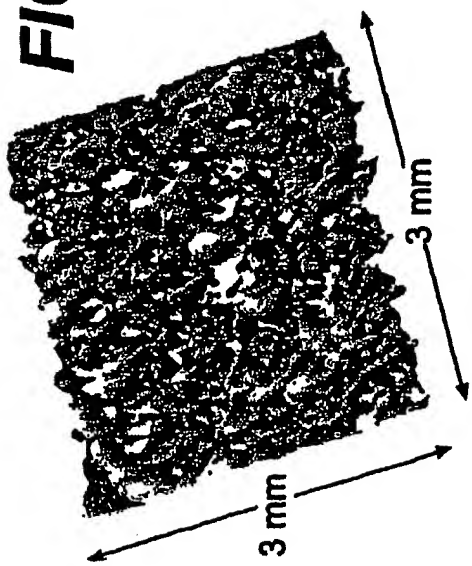
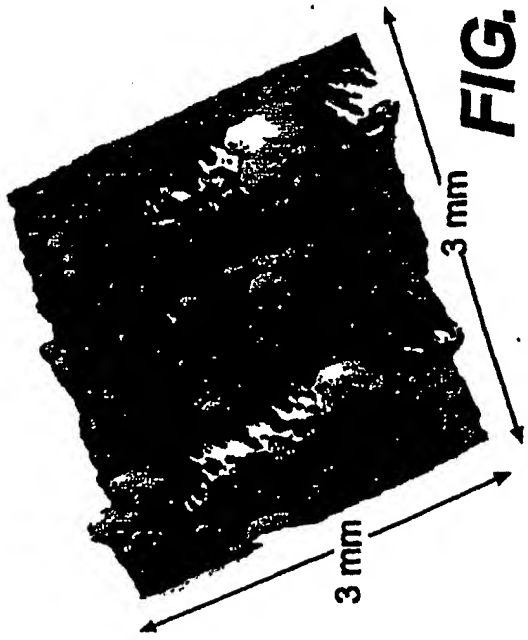


FIG. 18C



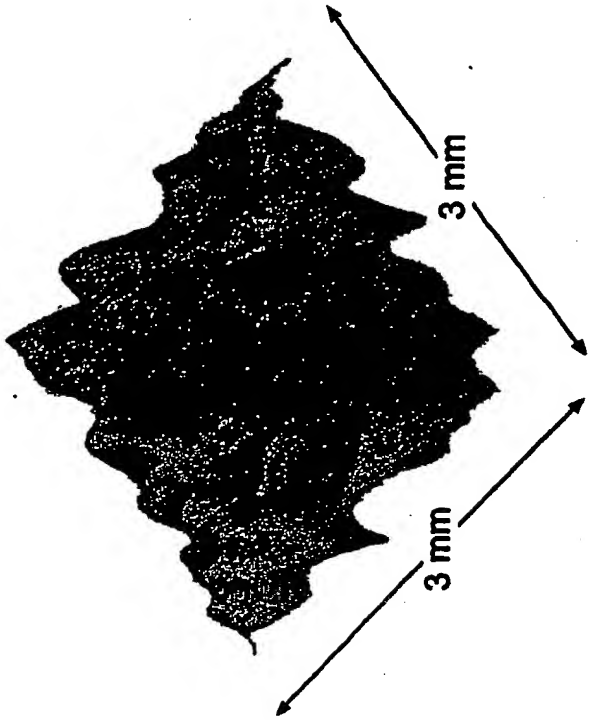


FIG. 19B

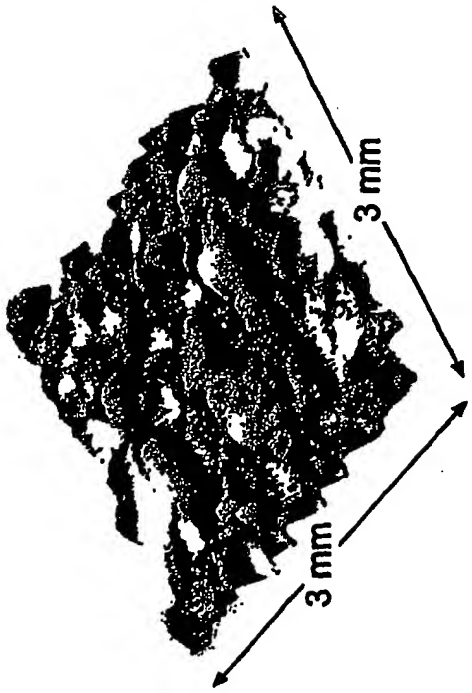


FIG. 19A

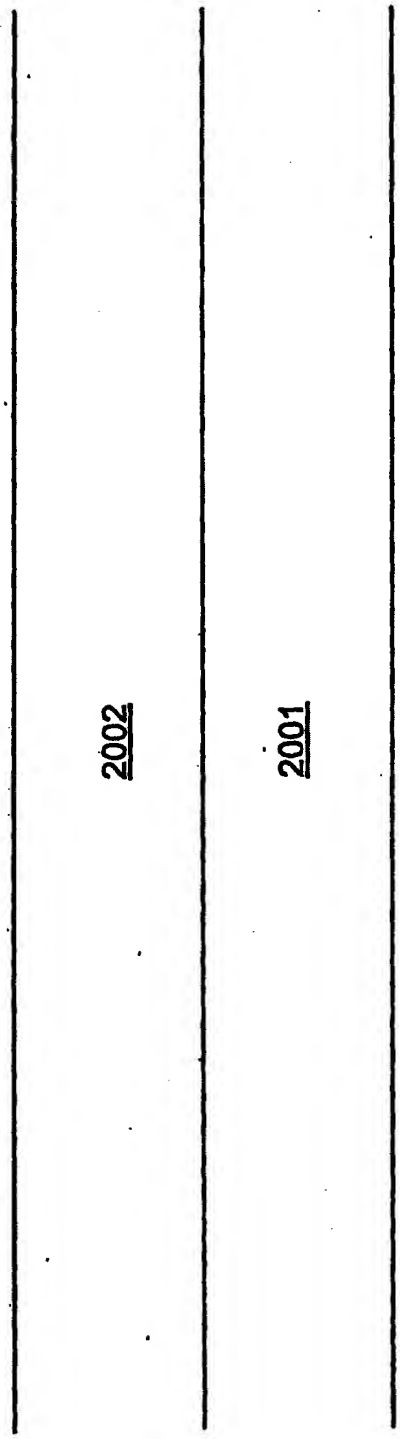


FIG. 20

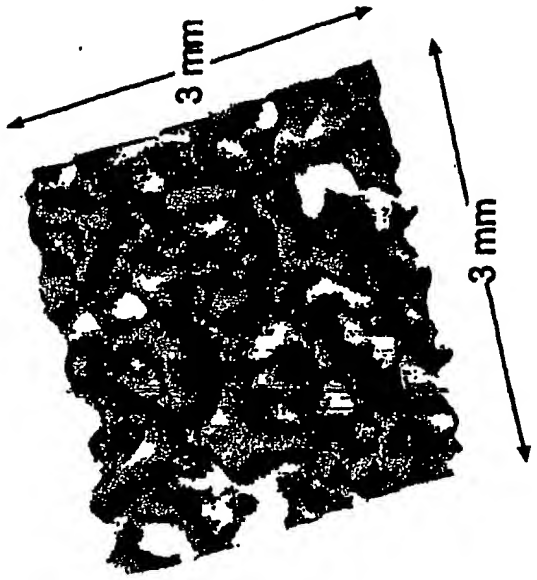


FIG. 21B

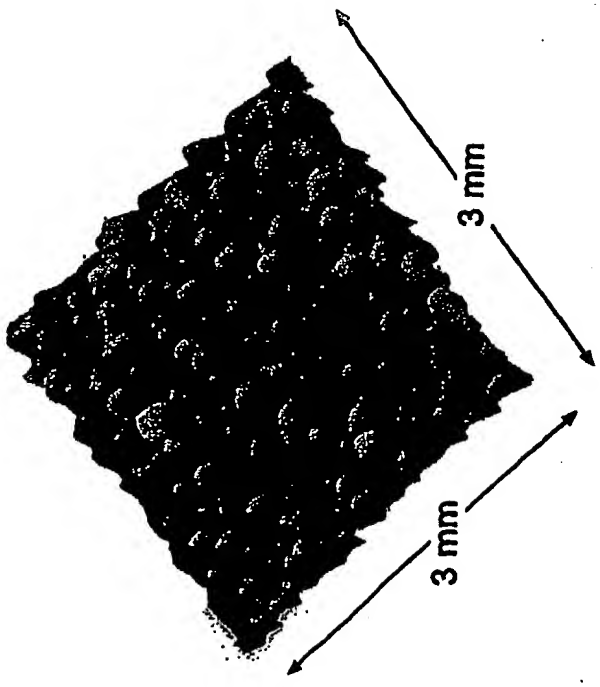


FIG. 21A

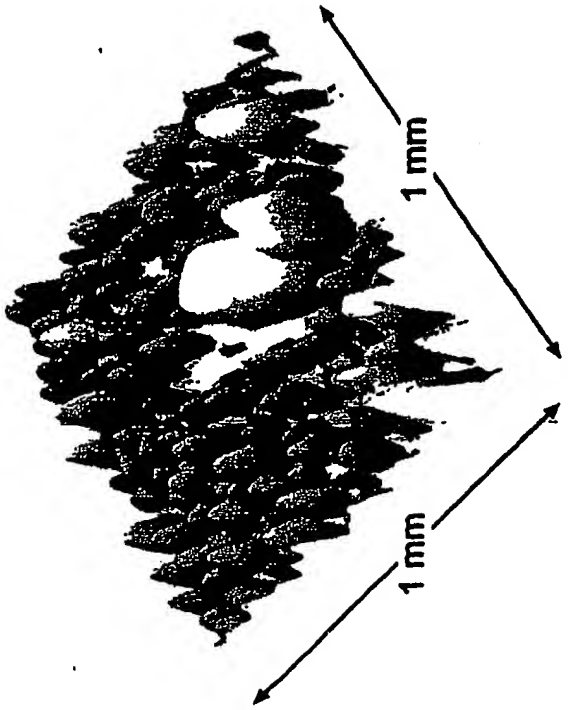


FIG. 22B

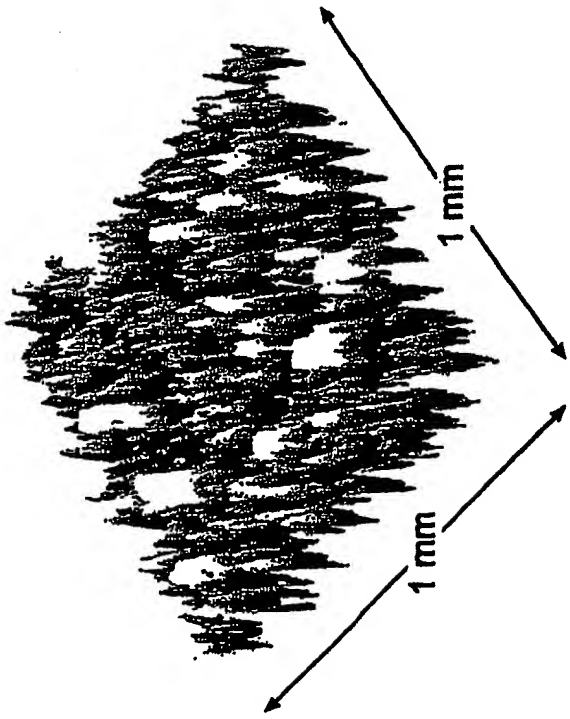


FIG. 22A

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(21) International Application Number:
PCT/US2004/005531

(22) International Filing Date: 26 February 2004 (26.02.2004)

(25) Filing Language: English

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(71) Applicants and
(72) Inventors: **NARASIMHAN, Mukundan** [IN/US]; 293 Bluefield Drive, San Jose, CA 91536 (US). **DEMARAY, Richard, E.** [US/US]; 190 Fawn Lane, Portola Valley, CA 94028 (US). **BROOKS, Peter** [US/US]; 611 Glen Alto Drive, Los Altos, CA 94024 (US).

(74) Agent: **GARRETT, Arthur, S.**; Finnegan, Henderson, Farabow Garrett & Dunner, L. L.P., 1300 I Street, N.W., Washington, DC 20005-3315 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
6 January 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 2004/077519 A3

(54) Title: DIELECTRIC BARRIER LAYER FILMS

(57) Abstract: In accordance with the present invention, a dielectric barrier layer is presented. A barrier layer according to the present invention includes a densified amorphous dielectric layer deposited on a substrate by pulsed-DC, substrate biased physical vapor deposition, wherein the densified amorphous dielectric layer is a barrier layer. A method of forming a barrier layer according to the present inventions includes providing a substrate and depositing a highly densified, amorphous, dielectric material over the substrate in a pulsed-dc, biased, wide target physical vapor deposition process. Further, the process can include performing a soft-metal breath treatment on the substrate. Such barrier layers can be utilized as electrical layers, optical layers, immunological layers, or tribological layers.

INTERNATIONAL SEARCH REPORT

International Application No
/US2004/005531

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 C23C14/34 C23C14/08 C23C14/58 H01L51/30 C23C14/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KIM J-Y ET AL: "Frequency-dependent pulsed direct current magnetron sputtering of titanium oxide films" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY A. VACUUM, SURFACES AND FILMS, AMERICAN INSTITUTE OF PHYSICS, NEW YORK, NY, US, vol. 19, no. 2, March 2001 (2001-03), pages 429-434, XP012005484 ISSN: 0734-2101 the whole document	1,3,4, 8-10,16, 17,21, 22,28, 39,40, 43,44

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 October 2004	25/10/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Patterson, A